FUP1 Ver : 2.1

USB to Audio PCM Processor for VoIP

Sep., 2006

General Description

Using a microphone & a speaker to engage a talk between two different locations over the internet is nowadays very popular, thanks to the deployment of broadband access infrastructure and Instant Messaging. The FUP1 provides a voice-over-the-internet solution that integrates telephony hardware to the Microsoft platform at low cost.

FUP1 is a USB to audio PCM bus processor for VoIP applications. The FUP1 is a fully USB spec v1.1 compatible interface which can be connected directly to the USB bus. And it implements USB audio class spec v1.0 that processes the serial USB interface to the specific audio PCM serial bus. Its Audio PCM bus can be connected to a SLIC or any audio codec IC. It also provides customized general interfaces for users & telephony functions.

The FUP1 is compatible with Microsoft USB audio device driver. **The string descriptor describing manufacture and product displays specific information of the USB audio device.**

In addition to audio, FUP1 supports device descriptor for MIC & SPK volume control and dual way audio recording control through wave in panel user interface.

The FUP1 supports configurable general I/Os for the telephony system integration such as Subscriber Line Interface (phone interface), USB phone, and Direct Access Arrangement to the telephone line applications.

Also, product ID (PID), vendor ID (VID), manufacture & product string descriptors can be set by EEPROM interface.

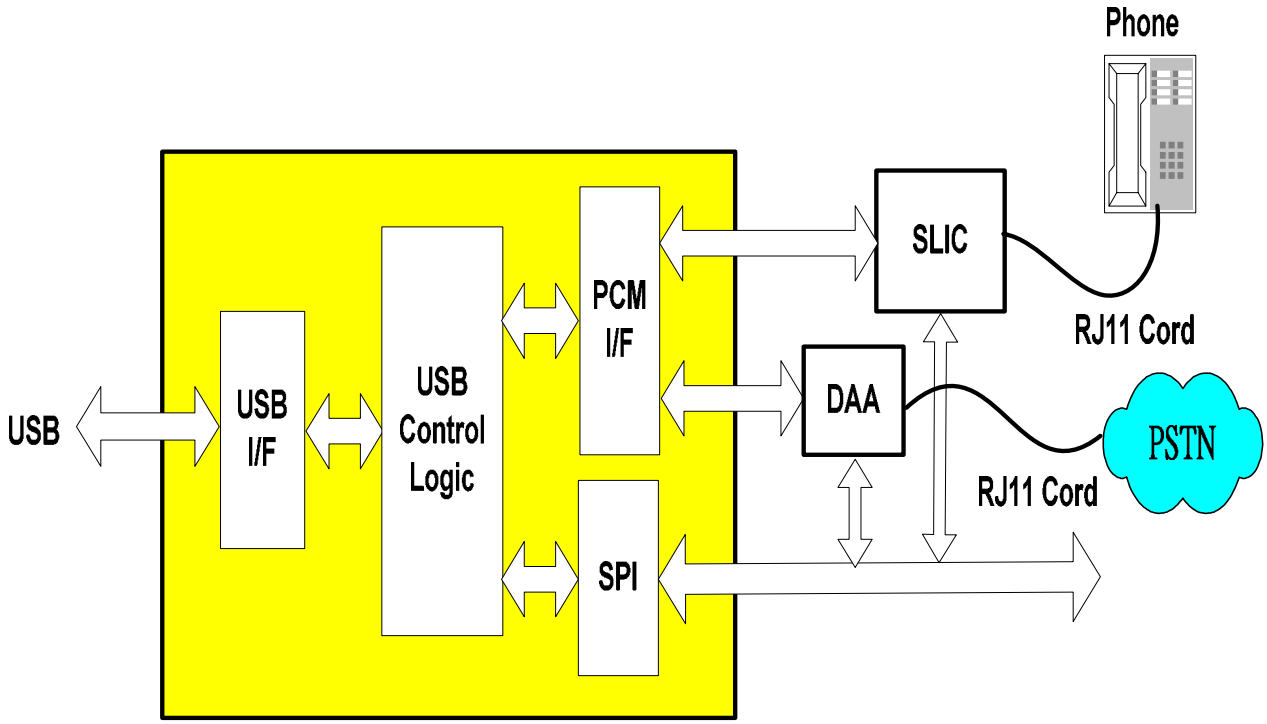
FUP1 supports dedicated configure pins for additional configuration management (Only supported by 100 pin PQFP package).

The FUP1 supports customer (CID) for specific applications.

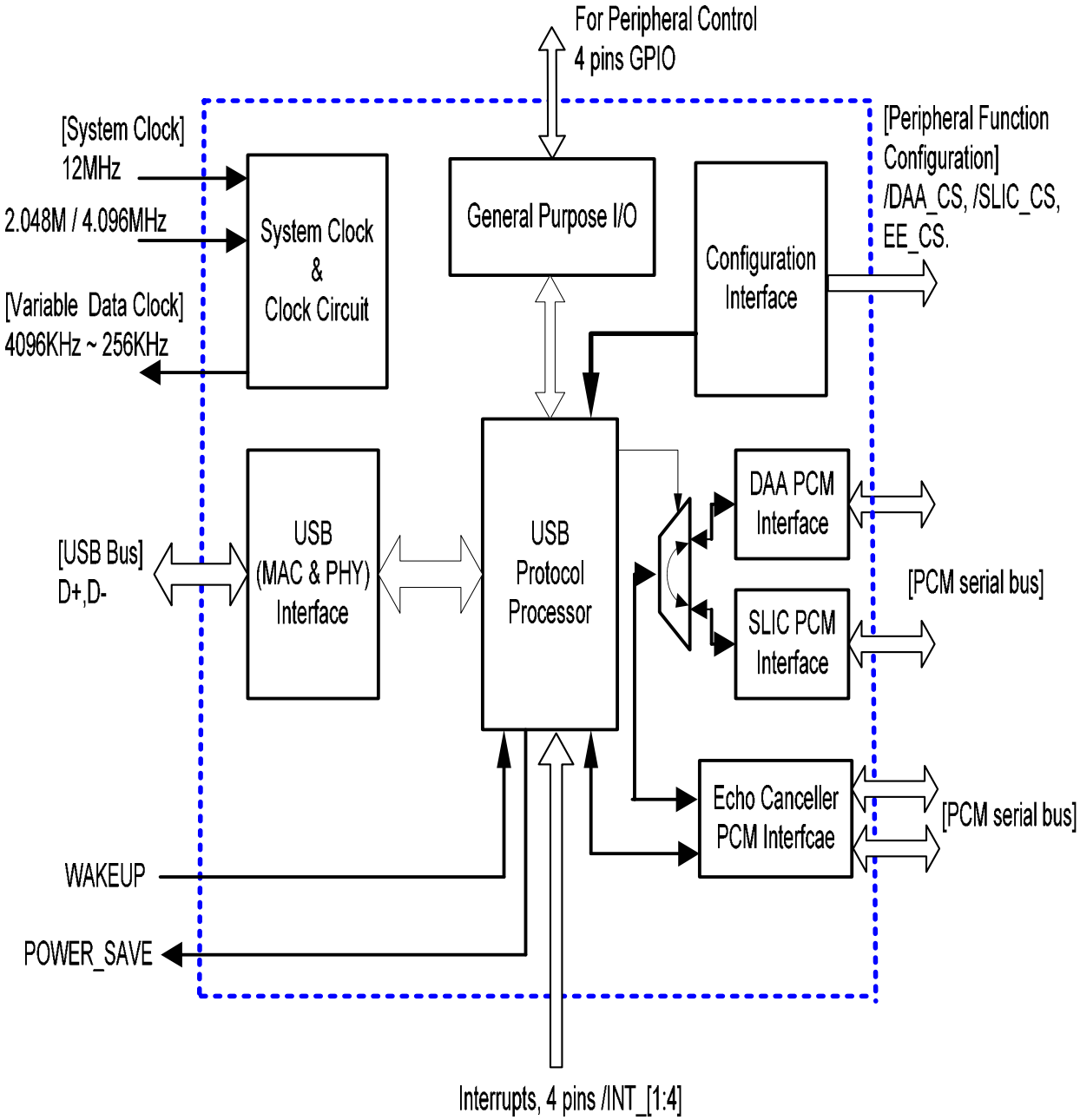
Features

- USB Spec v1.1 compliable, provide full speed 12Mbps USB transceiver and USB node with Control, Isochronous In/Out Endpoints.
- Support USB Audio Device Class Spec v1.0 with PCM serial bus interface.
- Support 4 GPIO pins for telephony system control.
- Support volume control and **dual way audio recording** control through wave in control panel user interface.
- Provide EEPROM interface for PID, VID, serial number, manufacture & product string descriptors.
- Support 4 configuration serial peripheral interfaces with chip select that can be connected simultaneously to such as EEPROM, and other peripheral interface applications.
- Support alternative serial SMBus bus for indirect configuration control through microcontroller.
- Compatible with Microsoft USB Audio Device driver & support USB HID Class command for device driver control.
- **Support customer ID (CID) for specific applications.**
- Support USB audio device class descriptor tables **with string descriptor describing manufacture and product information for the USB audio device.**
- Provide two PCM serial bus interfaces by control through multiplexer and PCM bus DIN/DOUT path return between different peripheral devices.
- **Support PCM16 to 8-bit A / μ-law translation.**
- Provide USB suspend and remote wake up (not supported by 48 pin LQFP package).
- Single 12MHz clock input with on-chip PLL.
- 3.3V power supply and **with 5V tolerance I/O**, 100 pin PQFP, 48 pin LQFP and 64 pin QFN package.

System Diagram



Block Diagram



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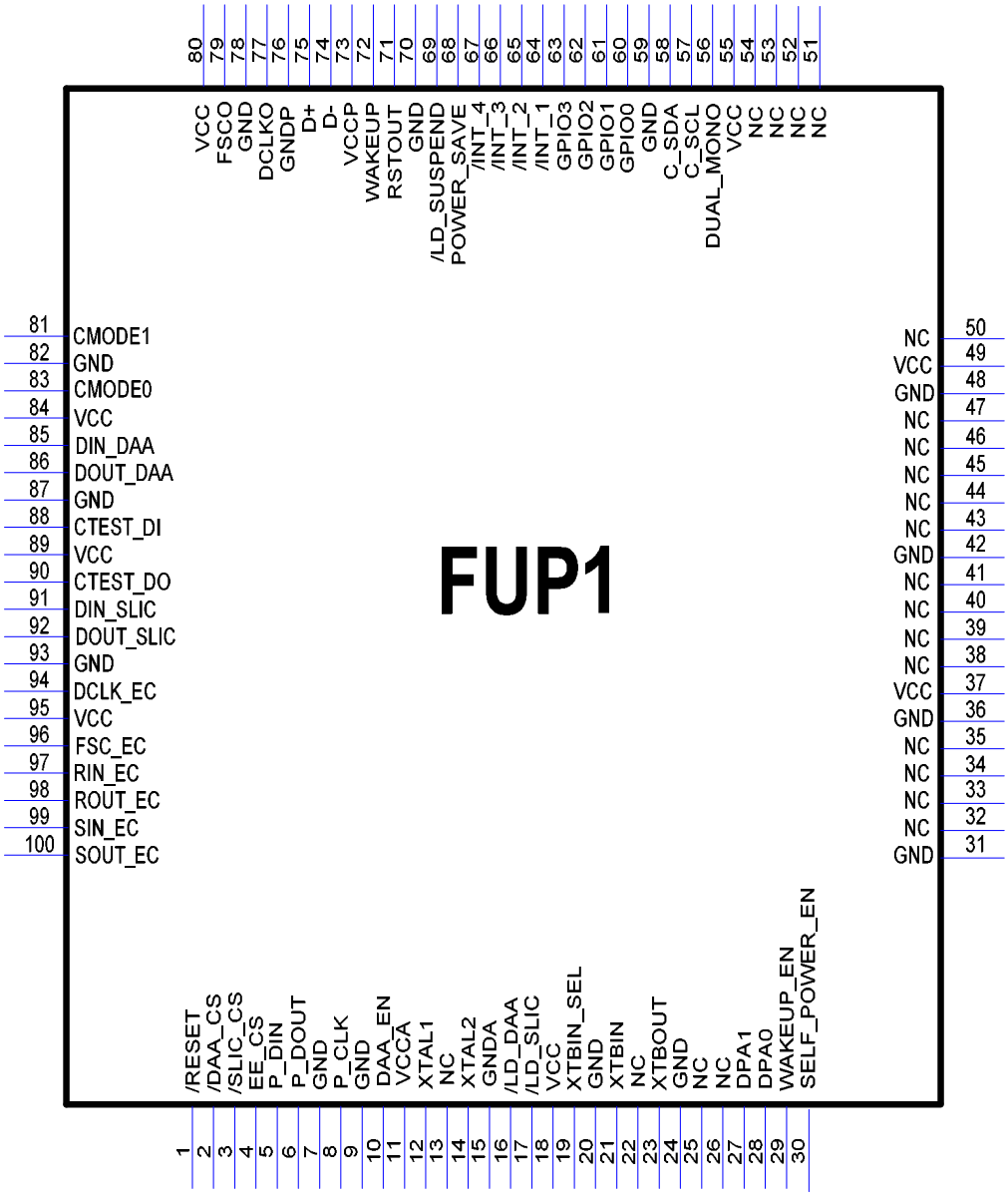
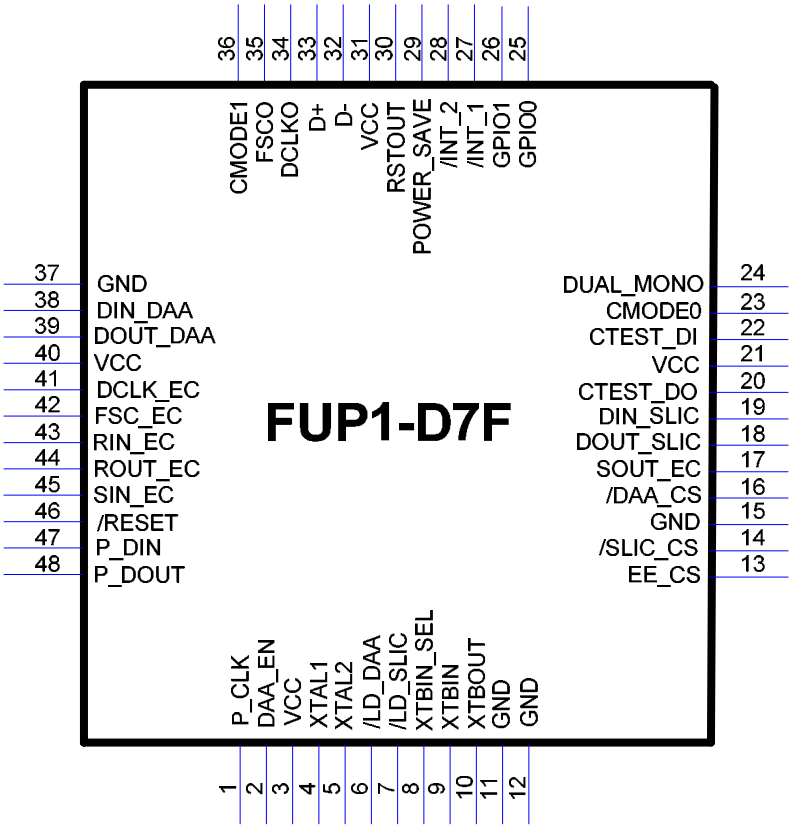


1.2 FUP1-D7F


FUP1-D7F
1 P_CLK
2 DAA_EN
3 VCC
4 XTAL1
5 XTAL2
6 /LD_DAA
7 /LD_SLIC
8 XTBIN_SEL
9 XTBIN
10 XTBOUT
11 GND
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35 FSCO
36 CMODE1
37 GND
38 DIN_DAA
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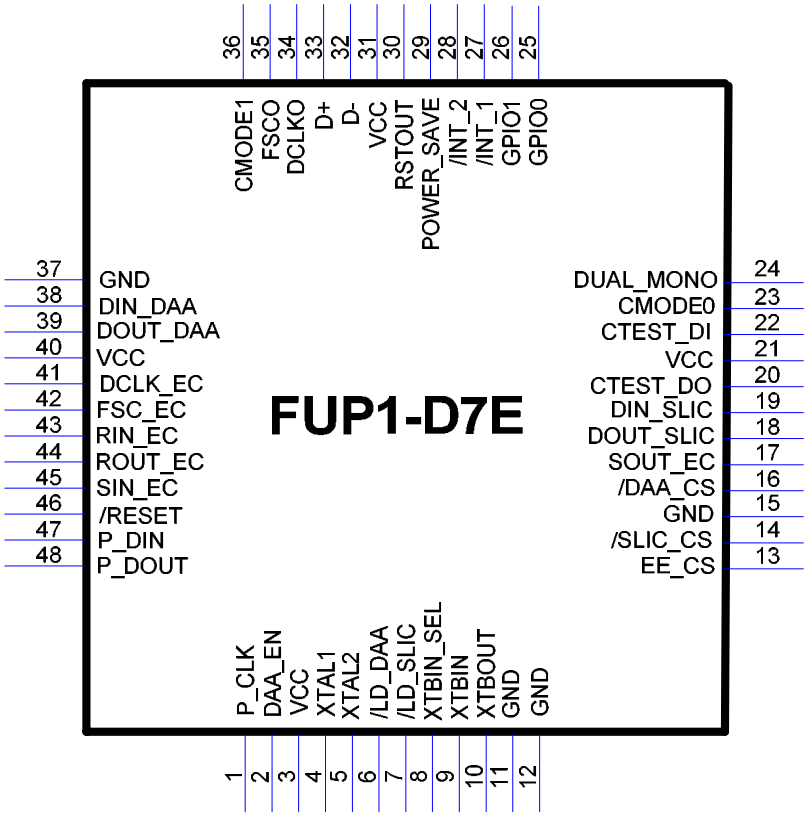
40 VCC
41 DCLK_EC
42 FSC_EC
43 RIN_EC
44 ROUT_EC
45 SIN_EC
46 /RESET
47 P_DIN
48 P_DOUT

1.3 FUP1-D7E


FUP1-D7E
1 P_CLK
2 DAA_EN
3 VCC
4 XTAL1
5 XTAL2
6 /LD_DAA
7 /LD_SLIC
8 XTBIN_SEL
9 XTBIN
10 XTBOUT
11 GND
12 GND
13 EE_CS
14 /SLIC_CS
15 GND
16 /DAA_CS
17 SOUT_EC
18 DOUT_SLIC
19 DIN_SLIC
20 CTEST_DO
21 VCC
22 CTEST_DI
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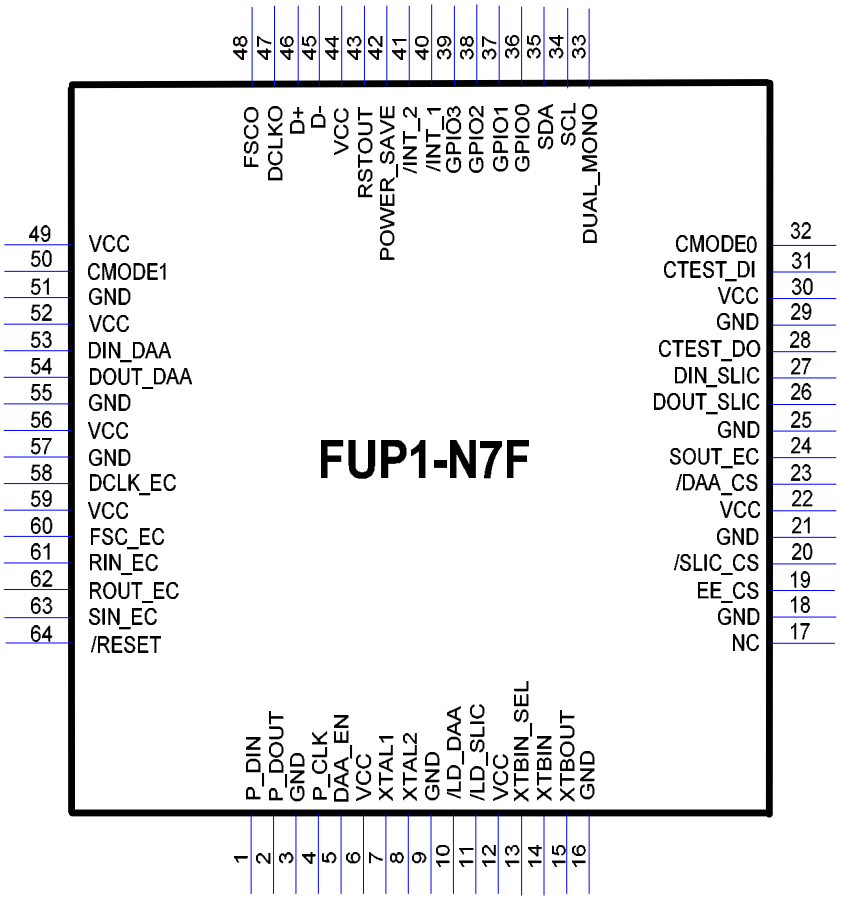
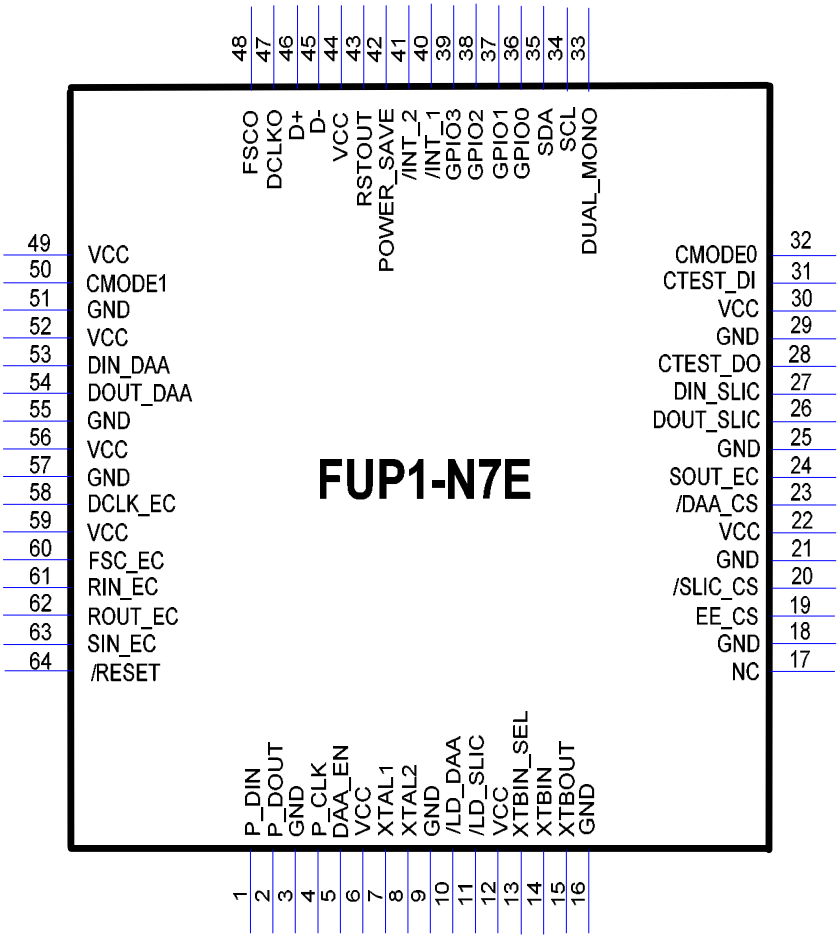
31 VCC
32 D-
33 D+
34 DCLKO
35 FSCO
36 CMODE1
37 GND
38 DIN_DAA
39 DOUT_DAA
40 VCC
41 DCLK_EC
42 FSC_EC
43 RIN_EC
44 ROUT_EC
45 SIN_EC
46 /RESET
47 P_DIN
48 P_DOUT

1.4 FUP1-N7F


FUP1-N7F
1 P_DIN
2 P_DOUT
3 GND
4 P_CLK
5 DAA_EN
6 VCC
7 XTAL1
8 XTAL2
9 GND
10 /LD_DAA
11 /LD_SLIC
12 VCC
13 XTBIN_SEL
14 XTBIN
15 XTBOUT
16 GND
17 NC
18 GND
19 EE_CS
20 /SLIC_CS
21 GND
22 VCC
23 /DAA_CS
24 SOUT_EC
25 GND
26 DOUT_SLIC
27 DIN_SLIC
28 CTEST_DO
29 GND
30 VCC
31 CTEST_DI
32 CMODE0
33 DUAL_MONO
34 SCL
35 SDA
36 GPIO0
37 GPIO1
38 GPIO2
39 GPIO3
40 /INT_1
41 /INT_2
42 POWER_SAVE
43 RSTOUT
44 VCC
45 D-
46 D+
47 DCLKO
48 FSCO
49 VCC
50 CMODE1
51 GND
52 VCC
53 DIN_DAA
54 DOUT_DAA
55 GND
56 VCC
57 GND
58 DCLK_EC
59 VCC
60 FSC_EC
61 RIN_EC
62 ROUT_EC
63 SIN_EC
64 /RESET

1.5 FUP1-N7E


FUP1-N7E
1 P_DIN
2 P_DOUT
3 GND
4 P_CLK
5 DAA_EN
6 VCC
7 XTAL1
8 XTAL2
9 GND
10 /LD_DAA
11 /LD_SLIC
12 VCC
13 XTBIN_SEL
14 XTBIN
15 XTBOUT
16 GND
17 NC
18 GND
19 EE_CS
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21 GND
22 VCC
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34 SCL
35 SDA
36 GPIO0
37 GPIO1
38 GPIO2
39 GPIO3
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41 /INT_2
42 POWER_SAVE
43 RSTOUT
44 VCC
45 D-
46 D+
47 DCLKO
48 FSCO
49 VCC
50 CMODE1
51 GND
52 VCC
53 DIN_DAA
54 DOUT_DAA
55 GND
56 VCC
57 GND
58 DCLK_EC
59 VCC
60 FSC_EC
61 RIN_EC
62 ROUT_EC
63 SIN_EC
64 /RESET

2.0 PIN DESCRIPTION

2.1 USB Physical Layer Interface Pins

2.1.1 FUP1

Signal Name	Type	Pin No	Description
D+	I/O	75	USB positive data line
D-	I/O	74	USB negative data line

2.1.2 FUP1-D7F/D7E

Signal Name	Type	Pin No	Description
D+	I/O	33	USB positive data line
D-	I/O	32	USB negative data line

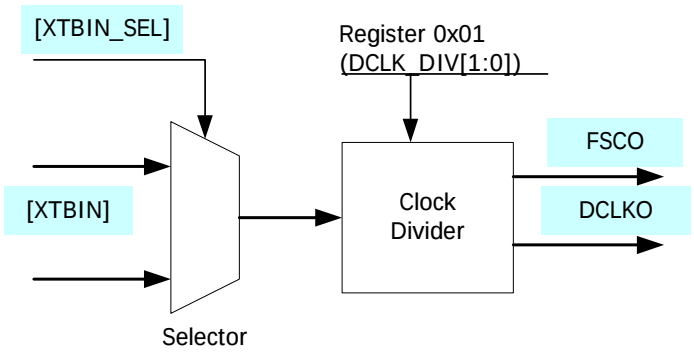
2.1.3 FUP1-N7F/N7E

Signal Name	Type	Pin No	Description
D+	I/O	46	USB positive data line
D-	I/O	45	USB negative data line

2.2 PCM Serial Bus Interface Pins (with 3.3V ~ 5V tolerance)

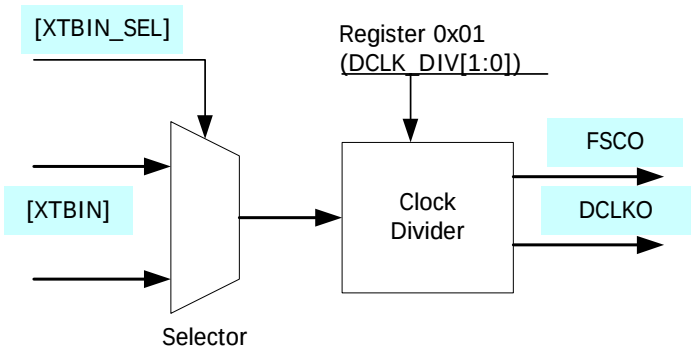
2.2.1 FUP1

Signal Name	Type	Pin No	Description
DIN_DAA	I, IPD	85	**PCM Serial Data Input from DAA :** PCM serial data input from DAA channel.
DIN_SLIC	I, IPD	91	**PCM Serial Data Input from SLIC :** PCM serial data input from SLIC channel.
DOUT_DAA	O/Z, 4mA	86	**PCM Serial Data Output to DAA :** PCM serial data output to DAA channel.
DOUT_SLIC	O/Z, 4mA	92	**PCM Serial Data Output to SLIC :** PCM serial data output to SLIC channel.
XTBIN_SEL	I, IPD	19	**XTBIN Input Select :** XTBIN is the source clock of internal clock divider. This allows XTBIN can be selected from different clock source. 0: when use 2048KHz OSC (default) 1: when use 4096KHz OSC
FSC_EC	I, IPD	96	**PCM Frame Synch Clock Input from Echo Canceller (EC) :** PCM frame synchronization 8KHz continuous clock input from Echo Canceller. This input can use either external frame synchronous signal or FSCO for PCM frame synchronization.
DCLK_EC	I, IPD	94	**PCM Data Clock Input from Echo Canceller (EC) :** PCM data clock input from Echo Canceller. This input can use either external data clock or DCLKO for variable data clock rate setting.
SOUT_EC	I, IPD	100	**PCM Transmit Data Input from Echo Canceller (EC) :** For echo cancellation, connect this pin to the transmit serial data output pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3.**
SIN_EC	O/Z, 4mA	99	**PCM Transmit Data Output to Echo Canceller (EC) :** For echo cancellation, connect this pin to the transmit serial data input pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.
ROUT_EC	I, IPD	98	**PCM Receive Data Input from Echo Canceller (EC) :** For echo cancellation, connect this pin to the receive serial data output pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.

Signal Name	Type	Pin No	Description
RIN_EC	O/Z, 4mA	97	**PCM Receive Data Output to Echo Canceller (EC) :** For echo cancellation, connect this pin to the receive serial data input pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.
FSCO	O, 8mA	79	**PCM Frame Synch Clock Output :** PCM port 1 or 2 frame synchronization 8KHz continuous clock output. It has 1-bit pulse width.
DCLKO	O, 8mA	77	**PCM Serial Data Clock :** PCM port 1 or 2 serial data clock output. Please refer to the DCLK_DIV[1:0] in the USB system control register 0x01 for variable clock rate configuration setting details. **Note For FSCO & DCLKO:** **When FSC & DCLK clock source are from XTBIN clock divider, the following diagram shows the logic block operation.** 
DUAL_MONO	I, IPD	56	**Audio Dual Mode Enable :** It is a power-on configuration pin to carry the audio dual or mono setting on FUP1. **Note :** **For detail, please refer to section 3.0.**

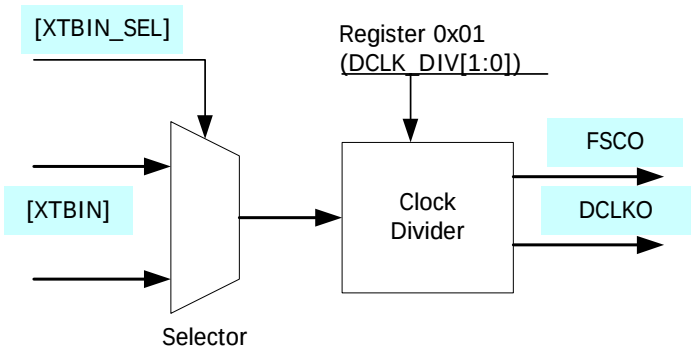
2.2.2 FUP1-D7F/D7E

Signal Name	Type	Pin No	Description
DIN_DAA	I, IPD	38	**PCM Serial Data Input from DAA :** PCM serial data input from DAA channel.
DIN_SLIC	I, IPD	19	**PCM Serial Data Input from SLIC :** PCM serial data input from SLIC channel.
DOUT_DAA	O/Z, 4mA	39	**PCM Serial Data Output to DAA :** PCM serial data output to DAA channel.
DOUT_SLIC	O/Z, 4mA	18	**PCM Serial Data Output to SLIC :** PCM serial data output to SLIC channel.
XTBIN_SEL	I, IPD	8	**XTBIN Input Select :** XTBIN is the source clock of internal clock divider. This allows XTBIN can be selected from different clock source. 0: when use 2048KHz OSC (default) 1: when use 4096KHz OSC
FSC_EC	I, IPD	42	**PCM Frame Synch Clock Input from Echo Canceller (EC) :** PCM frame synchronization 8KHz continuous clock input from Echo Canceller. This input can use either external frame synchronous signal or FSCO for PCM frame synchronization.
DCLK_EC	I, IPD	41	**PCM Data Clock Input from Echo Canceller (EC) :** PCM data clock input from Echo Canceller. This input can use either external data clock or DCLKO for variable data clock rate setting.
SOUT_EC	I, IPD	17	**PCM Transmit Data Input from Echo Canceller (EC) :** For echo cancellation, connect this pin to the transmit serial data output pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3.**
SIN_EC	O/Z, 4mA	45	**PCM Transmit Data Output to Echo Canceller (EC) :** For echo cancellation, connect this pin to the transmit serial data input pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.
ROUT_EC	I, IPD	44	**PCM Receive Data Input from Echo Canceller (EC) :** For echo cancellation, connect this pin to the receive serial data output pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.

Signal Name	Type	Pin No	Description
RIN_EC	O/Z, 4mA	43	**PCM Receive Data Output to Echo Canceller (EC) :** For echo cancellation, connect this pin to the receive serial data input pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.
FSCO	O, 8mA	35	**PCM Frame Synch Clock Output :** PCM port 1 or 2 frame synchronization 8KHz continuous clock output. It has 1-bit pulse width.
DCLKO	O, 8mA	34	**PCM Serial Data Clock :** PCM port 1 or 2 serial data clock output. Please refer to the DCLK_DIV[1:0] in the USB system control register 0x01 for variable clock rate configuration setting details. **Note For FSCO & DCLKO:** **When FSC & DCLK clock source are from XTBIN clock divider, the following diagram shows the logic block operation.** 
DUAL_MONO	I, IPD	24	**Audio Dual Mode Enable :** It is a power-on configuration pin to carry the audio dual or mono setting on FUP1-D7F/D7E. **Note :** **For detail, please refer to section 3.0.**

2.2.3 FUP1-N7F/N7E

Signal Name	Type	Pin No	Description
DIN_DAA	I, IPD	53	**PCM Serial Data Input from DAA :** PCM serial data input from DAA channel.
DIN_SLIC	I, IPD	27	**PCM Serial Data Input from SLIC :** PCM serial data input from SLIC channel.
DOUT_DAA	O/Z, 4mA	54	**PCM Serial Data Output to DAA :** PCM serial data output to DAA channel.
DOUT_SLIC	O/Z, 4mA	26	**PCM Serial Data Output to SLIC :** PCM serial data output to SLIC channel.
XTBIN_SEL	I, IPD	13	**XTBIN Input Select :** XTBIN is the source clock of internal clock divider. This allows XTBIN can be selected from different clock source. 0: when use 2048KHz OSC (default) 1: when use 4096KHz OSC
FSC_EC	I, IPD	60	**PCM Frame Synch Clock Input from Echo Canceller (EC) :** PCM frame synchronization 8KHz continuous clock input from Echo Canceller. This input can use either external frame synchronous signal or FSCO for PCM frame synchronization.
DCLK_EC	I, IPD	58	**PCM Data Clock Input from Echo Canceller (EC) :** PCM data clock input from Echo Canceller. This input can use either external data clock or DCLKO for variable data clock rate setting.
SOUT_EC	I, IPD	24	**PCM Transmit Data Input from Echo Canceller (EC) :** For echo cancellation, connect this pin to the transmit serial data output pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3.**
SIN_EC	O/Z, 4mA	63	**PCM Transmit Data Output to Echo Canceller (EC) :** For echo cancellation, connect this pin to the transmit serial data input pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.
ROUT_EC	I, IPD	62	**PCM Receive Data Input from Echo Canceller (EC) :** For echo cancellation, connect this pin to the receive serial data output pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.

Signal Name	Type	Pin No	Description
RIN_EC	O/Z, 4mA	61	**PCM Receive Data Output to Echo Canceller (EC) :** For echo cancellation, connect this pin to the receive serial data input pin of EC device. **Note :** **For detail connection diagram, please refer to section 6.3**.
FSCO	O, 8mA	48	**PCM Frame Synch Clock Output :** PCM port 1 or 2 frame synchronization 8KHz continuous clock output. It has 1-bit pulse width.
DCLKO	O, 8mA	47	**PCM Serial Data Clock :** PCM port 1 or 2 serial data clock output. Please refer to the DCLK_DIV[1:0] in the USB system control register 0x01 for variable clock rate configuration setting details. **Note For FSCO & DCLKO:** **When FSC & DCLK clock source are from XTBIN clock divider, the following diagram shows the logic block operation.** 
DUAL_MONO	I, IPD	33	**Audio Dual Mode Enable :** It is a power-on configuration pin to carry the audio dual or mono setting on FUP1-D7F/D7E. **Note :** **For detail, please refer to section 3.0.**

2.3 Miscellaneous

2.3.1 FUP1

Signal Name	Type	Pin No	Description
XTAL1	I	12	**Crystal Input :** External 12MHz (±100ppm) crystal connection. Used for system clock timing. It can be used an external 12MHz oscillator connected to XTAL1.
XTAL2	O	14	**Crystal Output :** External 12MHz crystal connection. Used for system clock timing. When using an external 12MHz oscillator connected to XTAL1, leave this pin unconnected.
/RESET	I, IPU	1	**System Reset :** It will receive a 500us reset pulse input. (Active low) < 100ms.
POWER_SAVE	O, 4mA	68	**Power Save :** Used to shut down external devices during USB bus is suspend.
/LD_SUSPEND	I/O, 8mA, IPD	69	**Suspend LED (Active Low) :** LED output to indicate the USB Suspend Mode 0: USB is in suspend mode. 1: USB is in normal operation.
WAKEUP	I, IPD	72	**Wakeup Event Input :** Set to this pin will generate a wakeup signal to the host computer. **Note:** To enable wakeup input at power on or reset, set PID [11] to 1.
XTBIN	I	21	**Oscillator Input :** PCM block clock divider source, 2048KHz or 4096KHz (±100ppm) selected by pin XTBIN_SEL.
XTBOUT	O	23	**Oscillator Output :** PCM block clock Output.
RSTOUT	O, 8mA	71	**External Device Reset Output :** It will output a reset pulse follows system reset or by software programmed and sent to all connected peripherals for 500us.
CMODE[1:0]	I, IPU	81,83	**Chip Mode Selection :** ***Should be left open in the normal operation.***
CTEST_DI	I, IPD	88	**Chip Test Data Input :** ***Should be left open in the normal operation.***
CTEST_DO	O, 4mA	90	**Chip Test Data Output :** ***Should be left open in the normal operation.***
DPA[1:0]	I, IPD	27, 28	**Device Power Allocation :** DPA1 DPA0 Selected Power 0 0 500mA Max. (default) 0 1 300mA Max. 1 0 200mA Max. 1 1 100mA Max.

Signal Name	Type	Pin No	Description
WAKEUP_EN	I, IPD	29	**USB Wakeup Function :** 0 : Don't support USB remote wakeup function. (default) 1 : Support USB remote wakeup function.
SELF_POWER_EN	I, IPD	30	**Self/Bus Power Input :** When power on or system reset, this pin will carry self or USB bus powered setting into the device. 0 : USB bus powered Input. (default) 1 : Self powered input.
GPIO[3:0]	I/O/Z 8mA, IPD	63~60	**General Purpose IO [3:0] :** These pins can be input or output for general purpose use. Through register 0x0A settings, each pin of GPIO can be programmed individually.
DAA_EN	O, 24mA	10	**DAA Enable :** This is a highly driving output especially for coil induced mechanism application. It is the direct output pin of DAA_EN bit of USB system control register 0x01.
/LD_DAA	I/O, 8mA, IPU	16	**DAA LED (Active Low) :** LED output to indicate the DAA is available and is controlled by the DAA_EN bit of USB system control register 0x01. 0: DAA is available. 1: DAA is not available.
/LD_SLIC	I/O, 8mA, IPU	17	**SLIC LED : (Active Low) :** LED output to indicate the SLIC is available and is controlled by the DAA_EN bit of USB system control register 0x01. 0: SLIC is available. 1: SLIC is not available.

2.3.2 FUP1-D7F/D7E

Signal Name	Type	Pin No	Description
XTAL1	I	4	**Crystal Input :** External 12MHz (±100ppm) crystal connection. Used for system clock timing. It can be used an external 12MHz oscillator connected to XTAL1.
XTAL2	O	5	**Crystal Output :** External 12MHz crystal connection. Used for system clock timing. When using an external 12MHz oscillator connected to XTAL1, leave this pin unconnected.
/RESET	I, IPU	46	**System Reset :** It will receive a 500us reset pulse input. (Active low) < 100ms.
POWER_SAVE	O, 4mA	29	**Power Save :** Used to shut down external devices during USB bus is suspend.
XTBIN	I	9	**Oscillator Input :** PCM block clock divider source, 2048KHz or 4096KHz (±100ppm) selected by pin XTBIN_SEL.
XTBOUT	O	10	**Oscillator Output :** PCM block clock Output.
RSTOUT	O, 8mA	30	**External Device Reset Output :** It will output a reset pulse follows system reset or by software programmed and sent to all connected peripherals for 500us.
CMODE[1:0]	I, IPU	36,23	**Chip Mode Selection :** **Should be left open in the normal operation.**
CTEST_DI	I, IPD	22	**Chip Test Data Input :** Should be left open in the normal operation.
CTEST_DO	O, 4mA	20	**Chip Test Data Output :** Should be left open in the normal operation.

Signal Name	Type	Pin No	Description
GPIO[1:0]	I/O/Z 8mA, IPD	26, 25	**General Purpose IO [3:0] :** These pins can be input or output for general purpose use. Through register 0x0A settings, each pin of GPIO can be programmed individually.
DAA_EN	O, 24mA	2	**DAA Enable :** This is a highly driving output especially for coil induced mechanism application. It is the direct output pin of DAA_EN bit of USB system control register 0x01.
/LD_DAA	I/O, 8mA, IPU	6	**DAA LED (Active Low) :** LED output to indicate the DAA is available and is controlled by the DAA_EN bit of USB system control register 0x01. 0: DAA is available. 1: DAA is not available.
/LD_SLIC	I/O, 8mA, IPU	7	**SLIC LED : (Active Low) :** LED output to indicate the SLIC is available and is controlled by the DAA_EN bit of USB system control register 0x01. 0: SLIC is available. 1: SLIC is not available.

2.3.3 FUP1-N7F/N7E

Signal Name	Type	Pin No	Description
XTAL1	I	7	**Crystal Input :** External 12MHz (±100ppm) crystal connection. Used for system clock timing. It can be used an external 12MHz oscillator connected to XTAL1.
XTAL2	O	8	**Crystal Output :** External 12MHz crystal connection. Used for system clock timing. When using an external 12MHz oscillator connected to XTAL1, leave this pin unconnected.
/RESET	I, IPU	64	**System Reset :** It will receive a 500us reset pulse input. (Active low) < 100ms.
POWER_SAVE	O, 4mA	42	**Power Save :** Used to shut down external devices during USB bus is suspend.
XTBIN	I	14	**Oscillator Input :** PCM block clock divider source, 2048KHz or 4096KHz (±100ppm) selected by pin XTBIN_SEL.
XTBOUT	O	15	**Oscillator Output :** PCM block clock Output.
RSTOUT	O, 8mA	43	**External Device Reset Output :** It will output a reset pulse follows system reset or by software programmed and sent to all connected peripherals for 500us.
CMODE[1:0]	I, IPU	50,32	**Chip Mode Selection :** **Should be left open in the normal operation.**
CTEST_DI	I, IPD	31	**Chip Test Data Input :** Should be left open in the normal operation.
CTEST_DO	O, 4mA	28	**Chip Test Data Output :** Should be left open in the normal operation.

Signal Name	Type	Pin No	Description
GPIO[3:0]	I/O/Z 8mA, IPD	39, 38, 37, 36	**General Purpose IO [3:0] :** These pins can be input or output for general purpose use. Through register 0x0A settings, each pin of GPIO can be programmed individually.
DAA_EN	O, 24mA	5	**DAA Enable :** This is a highly driving output especially for coil induced mechanism application. It is the direct output pin of DAA_EN bit of USB system control register 0x01.
/LD_DAA	I/O, 8mA, IPU	10	**DAA LED (Active Low) :** LED output to indicate the DAA is available and is controlled by the DAA_EN bit of USB system control register 0x01. 0: DAA is available. 1: DAA is not available.
/LD_SLIC	I/O, 8mA, IPU	11	**SLIC LED : (Active Low) :** LED output to indicate the SLIC is available and is controlled by the DAA_EN bit of USB system control register 0x01. 0: SLIC is available. 1: SLIC is not available.

2.4 Peripheral Configuration Interface Pins

2.4.1 FUP1

Signal Name	Type	Pin No	Description
/DAA_CS	O, 4mA	2	**DAA Serial Peripheral Interface Chip Select (Low Active) :** This pin can be used as a serial peripheral interface bus chip selection for the DAA device which is selected by SPI_DAA_EN bit in the USB system control register 0x01.
/SLIC_CS	O, 4mA	3	**SLIC Serial Peripheral Interface Chip Select (Low Active) :** This pin can be used as a serial peripheral interface bus chip selection for the SLIC device which is selected by SPI_SLIC_EN bit in the USB system control register 0x01.
EE_CS	I/O, 4mA, IPD	4	**Serial EEPROM Chip Select :** Asserted by the FUP1 to enable the external serial EEPROM (SPI type).
P_CLK	O, 4mA	8	**Peripheral Configuration Interface Data Clock Output :** This pin can be used as a serial control interface bus data clock for EEPROM, SLIC & DAA..
P_DIN	O/Z, 4mA	5	**Peripheral Configuration Interface Data Input :** This pin can be used as a serial control interface bus data from FUP1 to EEPROM, SLIC & DAA.
P_DOUT	I, IPD	6	**Peripheral Configuration Interface Data Output :** This pin can be used as a serial control interface bus data from EEPROM, SLIC & DAA to FUP1.
/INT_1	I, IPU	64	**Interrupt Input 1 (Low Active) :** This is an interrupt input from peripheral device.
/INT_2	I, IPU	65	**Interrupt Input 2 (Low Active) :** This is an interrupt input from peripheral device.
/INT_3	I, IPU	66	**Interrupt Input 3 (Low Active) :** This is an interrupt input from peripheral device.
/INT_4	I, IPU	67	**Interrupt Input 4 (Low Active) :** This is an interrupt input from peripheral device.

2.4.2 FUP1-D7F/D7E

Signal Name	Type	Pin No	Description
/DAA_CS	O, 4mA	16	**DAA Serial Peripheral Interface Chip Select (Low Active) :** This pin can be used as a serial peripheral interface bus chip selection for the DAA device which is selected by SPI_DAA_EN bit in the USB system control register 0x01.
/SLIC_CS	O, 4mA	14	**SLIC Serial Peripheral Interface Chip Select (Low Active) :** This pin can be used as a serial peripheral interface bus chip selection for the SLIC device which is selected by SPI_SLIC_EN bit in the USB system control register 0x01.
EE_CS	I/O, 4mA, IPD	13	**Serial EEPROM Chip Select :** Asserted by the FUP1 to enable the external serial EEPROM (SPI type).
P_CLK	O, 4mA	1	**Peripheral Configuration Interface Data Clock Output :** This pin can be used as a serial control interface bus data clock for EEPROM, SLIC & DAA..
P_DIN	O/Z, 4mA	47	**Peripheral Configuration Interface Data Input :** This pin can be used as a serial control interface bus data from FUP1 to EEPROM, SLIC & DAA.
P_DOUT	I, IPD	48	**Peripheral Configuration Interface Data Output :** This pin can be used as a serial control interface bus data from EEPROM, SLIC & DAA to FUP1.
/INT_1	I, IPU	27	**Interrupt Input 1 (Low Active) :** This is an interrupt input from peripheral device.
/INT_2	I, IPU	28	**Interrupt Input 2 (Low Active) :** This is an interrupt input from peripheral device.

2.4.3 FUP1-N7F/N7E

Signal Name	Type	Pin No	Description
/DAA_CS	O, 4mA	23	**DAA Serial Peripheral Interface Chip Select (Low Active) :** This pin can be used as a serial peripheral interface bus chip selection for the DAA device which is selected by SPI_DAA_EN bit in the USB system control register 0x01.
/SLIC_CS	O, 4mA	20	**SLIC Serial Peripheral Interface Chip Select (Low Active) :** This pin can be used as a serial peripheral interface bus chip selection for the SLIC device which is selected by SPI_SLIC_EN bit in the USB system control register 0x01.
EE_CS	I/O, 4mA, IPD	19	**Serial EEPROM Chip Select :** Asserted by the FUP1 to enable the external serial EEPROM (SPI type).
P_CLK	O, 4mA	4	**Peripheral Configuration Interface Data Clock Output :** This pin can be used as a serial control interface bus data clock for EEPROM, SLIC & DAA..
P_DIN	O/Z, 4mA	1	**Peripheral Configuration Interface Data Input :** This pin can be used as a serial control interface bus data from FUP1 to EEPROM, SLIC & DAA.
P_DOUT	I, IPD	2	**Peripheral Configuration Interface Data Output :** This pin can be used as a serial control interface bus data from EEPROM, SLIC & DAA to FUP1.
/INT_1	I, IPU	40	**Interrupt Input 1 (Low Active) :** This is an interrupt input from peripheral device.
/INT_2	I, IPU	41	**Interrupt Input 2 (Low Active) :** This is an interrupt input from peripheral device.

2.5 FUP1 CPU System Management Bus Pins

2.5.1 FUP1

Signal Name	Type	Pin No	Description
C_SDA	I/OD/Z, IPU	58	**SMBus Data I/O:** When SMBus is used, FUP1 is always a master device, so this is a slave device management serial bus data I/O and can be connected to a CPU.
C_SCL	I/OD/Z, IPU	57	**SMBus Data Clock:** When SMBus is used, FUP1 is always a master device, so this is a slave device management serial bus data clock and can be connected to a CPU.

2.5.2 FUP1-N7F/N7E

Signal Name	Type	Pin No	Description
C_SDA	I/OD/Z, IPU	35	**SMBus Data I/O:** When SMBus is used, FUP1 is always a master device, so this is a slave device management serial bus data I/O and can be connected to a CPU.
C_SCL	I/OD/Z, IPU	34	**SMBus Data Clock:** When SMBus is used, FUP1 is always a master device, so this is a slave device management serial bus data clock and can be connected to a CPU.

2.6 Power, Ground & NC Pins

2.6.1 FUP1

Signal Name	Type	Pin No	Description
VCC	P/G	18,37,49, 55,80,84, 89,95	3.3V for Digital Circuitry.
GND	P/G	7,9,15, 20,24,31, 36,42,48, 59,70,78, 82,87,93	Ground for Digital Circuitry.
VCCA	P/G	11	3.3V for Analog PLL Circuitry.
GNDA	P/G	15	Ground for Analog PLL Circuitry.
VCCP	P/G	73	3.3V for Analog USB 1.1 Transceiver.
GNDP	P/G	76	Ground for Analog USB 1.1 Transceiver.
NC		13, 22, 25,26,32, 33,34,35, 38,39,40, 41,43,44, 45,46,47, 50,51,52, 53,54	Not Connected

2.6.2 FUP1-D7F/D7E

Signal Name	Type	Pin No	Description
VCC	P/G	3,21,31, 40	3.3V for Digital Circuitry.
GND	P/G	11,12,15, 37	Ground for Digital Circuitry.

2.6.3 FUP1-N7F/N7E

Signal Name	Type	Pin No	Description
VCC	P/G	6,12,22, 30,44,49, 52,56,59	3.3V for Digital Circuitry.
GND	P/G	3,9,16,18 21,25,29, 51,55,57	Ground for Digital Circuitry.

2.7 Pin Type Designation

Pin Type	Description
I	Input buffer.
O	Output buffer, driven high or low at all times.
I/O/Z	Bi-directional buffer with high-impedance output.
O/Z	Output buffer with high-impedance capability.
4mA	Output low drive: 4 mA.
8mA	Output medium/low drive: 8 mA.
24mA	Output high drive: 24mA
IPU	Internal 75K Ohm pull-up
IPD	Internal 75K Ohm pull-down
P/G	Power / Ground

***Note:** When pull-up, please use a 1.2K pull-up resistor for protection instead of directly connecting to VCC. If you directly connect input pin to VCC and forget to connect FUP1's power pins to VCC plane, internal protection diode will turn on and sink-in a lot of current which may burn out I/O cell. Although it's a rear case, but it happens

3.0 POWER-ON SETTINGS

Configuration pins shown in the table below must be pulled up or down externally at reset to select the desired operational parameter. The recommended value of the pull-up/down resistors is 1.2K ohms.

3.1 FUP1

Pin Name	FUP1 Pin #	Configuration Description
DPA1	**27**	**Device Power Allocation :** DPA1 DPA0 Selected Power 0 0 500mA Max. (default) 0 1 300mA Max. 1 0 200mA Max. 1 1 100mA Max.
DPA0	**28**	
WAKEUP_EN	**29**	**USB Wakeup Function :** 0 : Don't support USB remote wakeup function. (default) 1 : Support USB remote wakeup function.
SELF_POWER_EN	**30**	**Self/Bus Power Input :** When power on or system reset, this pin will carry self or USB bus powered setting into the device. 0 : USB bus powered Input. (default) 1 : Self powered input.
EE_CS	**4**	**EEPROM Type Select :** It is a power-on configuration pin to carry the EEPROM type selection on FUP1. 0 : EEPROM type is SPI (default). 1 : EEPROM type is I^2C. **Note : 1. For the EEPROM of I^2C type, only the 1 byte register addressing mode is supported by the SMBus Control Register 0x09h.** **2. The SLA for the EEPROM of I^2C type is fixed on 1010000b**.
.DUAL_MONO	**56**	**Audio Dual Mode Enable :** It is a power-on configuration pin to carry the audio dual or mono setting on FUP1. 0 : Disable audio dual mode. (default is mono) 1 : Enable audio dual mode. **Note** : Set this pin to logic one, the device support dual-way audio wave in streams to the host, but the audio wave out loop back path is controlled by the Audio Control Register, 0x10, bit 6. It must be set to logic one to turn on the audio wave out loop back path to interleave with the normal mono wave in streams to form a dual-way audio streams to the host, otherwise, a dual-way wave in streams are interleaved with the silence and normal mono wave in streams to the host.

3.2 FUP1-D7F/D7E

Pin Name	FUP1 Pin #	Configuration Description
.DUAL_MONO	24	**Audio Dual Mode Enable :** It is a power-on configuration pin to carry the audio dual or mono setting on FUP1-D7F/D7E. 0 : Disable audio dual mode. (default is mono) 1 : Enable audio dual mode. **Note** : Set this pin to logic one, the device support dual-way audio wave in streams to the host, but the audio wave out loop back path is controlled by the Audio Control Register, 0x10, bit 6. It must be set to logic one to turn on the audio wave out loop back path to interleave with the normal mono wave in streams to form a dual-way audio streams to the host, otherwise, a dual-way wave in streams are interleaved with the silence and normal mono wave in streams to the host.

3.3 FUP1-N7F/N7E

Pin Name	FUP1 Pin #	Configuration Description
EE_CS	19	**EEPROM Type Select :** It is a power-on configuration pin to carry the EEPROM type selection on FUP1. 0 : EEPROM type is SPI (default). 1 : EEPROM type is I^2C. **Note : 1. For the EEPROM of I^2C type, only the 1 byte register addressing mode is supported by the SMBus Control Register 0x09h.** **2. The SLA for the EEPROM of I^2C type is fixed on 1010000b**.
.DUAL_MONO	33	**Audio Dual Mode Enable :** It is a power-on configuration pin to carry the audio dual or mono setting on FUP1-D7F/D7E. 0 : Disable audio dual mode. (default is mono) 1 : Enable audio dual mode. **Note** : Set this pin to logic one, the device support dual-way audio wave in streams to the host, but the audio wave out loop back path is controlled by the Audio Control Register, 0x10, bit 6. It must be set to logic one to turn on the audio wave out loop back path to interleave with the normal mono wave in streams to form a dual-way audio streams to the host, otherwise, a dual-way wave in streams are interleaved with the silence and normal mono wave in streams to the host.

4.0 REGISTERS & EEPROM

FUP1's internal registers are mapped from address 0x00 to 0x1C and are accessed through USB end point by USB device driver. And 4 GPIO pins can each be programmed through registers 0x0A.

4.1 Internal Registers: 0x00h ~ 0x1D

4.1.1 System Control Register

1. FUP1/FUP1-D7F/D7E/N7F/N7E USB System Control Register, 0x00h

Bit	Type	R/W	Description
7~6	Reserved	RO	
5	**SRESET_EN**	R/W, SC	**Software System Reset Enable :** 0 : Normal Operation (default). 1 : Reset FUP1 for 500us. **Note :** **It will be self-clear after the end of the reset pulse.**
4	**USB_PATH**	R/W	**USB Pathway Select :** 0 : From USB to DAA PCM bus (default). 1 : From USB to SLIC PCM bus.
3	**PCM_LP1**	R/W	**PCM Loop Path 1 :** 0 : Disable PCM Loop Path 1 (default). 1 : From DAA PCM TX switch to SLIC PCM RX
2	**PCM_LP2**	R/W	**PCM Loop Path 2 :** 0 : Disable PCM Loop Path 2 (default). 1 : From SLIC PCM TX switch to DAA PCM RX.
1	**RSTOUT_EN**	R/W, SC	**External Device Reset Output Enable :** 0 : RSTOUT pin is idle (inactive). 1 : Assert RSTOUT pin a reset pulse of 500us period **Note :** **1. The reset pulse polarity can be controlled by RSTOUT_LOW bit (bit 0).** **2. It will be self-clear after the end of reset pulse.**
0	**RSTOUT_LOW**	R/W	**RSTOUT Low Active :** (for peripheral device reset) 0: RSTOUT is low active (default). 1: RSTOUT is high active.

2. FUP1/FUP1-N7F/N7E USB System Control Register, 0x01h

Bit	Type	R/W	Description
7	**GPIO3_AFE**	R/W	**GPIO3 Alternate Function Enable :** 0 : Disable the alternate function of GPIO3 pin (Default). 1 : Enable the alternate function of GPIO3 pin to act as /AUX_CS, the chip select of the Auxiliary Serial Peripheral Interface for the specific application such as caller ID module.
6	**SPI_AUX_EN**	R/W	**Auxiliary Serial Peripheral Interface Enable :** 0 : Auxiliary Serial Peripheral Interface is rejected (default). 1 : Auxiliary Serial Peripheral Interface is selected. **Note : If this auxiliary SPI is selected, then other mutual exclusive SPI control bits, such as SPI_SLIC_EN & SPI_DAA_EN must be set to rejected.**
5	**DAA_EN**	R/W	**DAA Enable :** 0 : SLIC is selected. 1 : DAA is selected (default). **Note:** 1. DAA_EN can be a highly driving current output pin for specific purpose use. 2. It is also a DAA / SLIC select output pin only.
4	**RESERVED**	RO	**Must be kept as logic "0".**
3	**SPI_SLIC_EN**	R/W	**SLIC Serial Peripheral Interface Enable :** 0 : SLIC Serial Peripheral Interface is rejected (default). 1 : SLIC Serial Peripheral Interface is selected. **Note : If this SLIC SPI is selected, then other mutual exclusive SPI control bits, such as SPI_AUX_EN & SPI_DAA_EN must be set to rejected.**
2	**SPI_DAA_EN**	R/W	**DAA Serial Peripheral Interface Enable :** 0 : DAA Serial Peripheral Interface is rejected (default). 1 : DAA Serial Peripheral Interface is selected. **Note : If this DAA SPI is selected, then other mutual exclusive SPI control bits, such as SPI_AUX_EN & SPI_SLIC_EN must be set to rejected.**
1	**DCLK_DIV1**	R/W	**PCM Data Clock Divider: (for pin "DCLKO) :** Setting for DCLKO data clock divider. **DCLK_DIV[1:0]** (If OSC 2048KHz is used) 0: = XTBIN／1 ; 2048KHz (default) 1: = XTBIN／2 ;1024KHz 2: = XTBIN／4 ; 512KHz 3: = XTBIN／8 ; 256KHz
0	**DCLK_DIV0**	R/W	

3. FUP1-D7F/D7E USB System Control Register, 0x01h

Bit	Type	R/W	Description
7	**GPIO1_AFE**	R/W	**GPIO1 Alternate Function Enable :** 0 : Disable the alternate function of GPIO1 pin (Default). 1 : Enable the alternate function of GPIO1 pin to act as /AUX_CS, the chip select of the Auxiliary Serial Peripheral Interface for the specific application such as caller ID module.
6	**SPI_AUX_EN**	R/W	**Auxiliary Serial Peripheral Interface Enable :** 0 : Auxiliary Serial Peripheral Interface is rejected (default). 1 : Auxiliary Serial Peripheral Interface is selected. **Note : If this auxiliary SPI is selected, then other mutual exclusive SPI control bits, such as SPI_SLIC_EN & SPI_DAA_EN must be set to rejected.**
5	**DAA_EN**	R/W	**DAA Enable :** 0 : SLIC is selected. 1 : DAA is selected (default). **Note:** 1. DAA_EN can be a highly driving current output pin for specific purpose use. 2. It is also a DAA / SLIC select output pin only.
4	**RESERVED**	R/W	**Must be kept as logic "0".**
3	**SPI_SLIC_EN**	R/W	**SLIC Serial Peripheral Interface Enable :** 0 : SLIC Serial Peripheral Interface is rejected (default). 1 : SLIC Serial Peripheral Interface is selected. **Note : If this SLIC SPI is selected, then other mutual exclusive SPI control bits, such as SPI_AUX_EN & SPI_DAA_EN must be set to rejected.**
2	**SPI_DAA_EN**	R/W	**DAA Serial Peripheral Interface Enable :** 0 : DAA Serial Peripheral Interface is rejected (default). 1 : DAA Serial Peripheral Interface is selected. **Note : If this DAA SPI is selected, then other mutual exclusive SPI control bits, such as SPI_AUX_EN & SPI_SLIC_EN must be set to rejected.**
1	**DCLK_DIV1**	R/W	**PCM Data Clock Divider (for pin "DCLKO) :** Setting for DCLKO data clock divider. **DCLK_DIV[1:0]** (If OSC 2048KHz is used) 0: = XTBIN／1 ; 2048KHz (default) 1: = XTBIN／2 ;1024KHz 2: = XTBIN／4 ; 512KHz 3: = XTBIN／8 ; 256KHz
0	**DCLK_DIV0**	R/W	

4.1.2 SMBus Control Register

1. FUP1/FUP1-N7F/N7E SMBus 1st Data Register, 0x02h

Bit	Type	R/W	Description
7	**SMB1_D7**	R/W	**1st Byte Data of SMBus :** When write operation, SMB1_D[7:0] are sent to CPU through SMBus. When read operation, SMB1_D[7:0] are received from CPU through SMBus.
6	**SMB1_D6**	R/W	
5	**SMB1_D5**	R/W	
4	**SMB1_D4**	R/W	
3	**SMB1_D3**	R/W	
2	**SMB1_D2**	R/W	
1	**SMB1_D1**	R/W	
0	**SMB1_D0**	R/W	

2. FUP1/FUP1-N7F/N7E SMBus 2nd Data Register, 0x03h

Bit	Type	R/W	Description
7	**SMB2_D7**	R/W	**2nd Byte Data of SMBus :** When write operation, SMB2_D[7:0] are sent to CPU through SMBus. When read operation, SMB2_D[7:0] are received from CPU through SMBus.
6	**SMB2_D6**	R/W	
5	**SMB2_D5**	R/W	
4	**SMB2_D4**	R/W	
3	**SMB2_D3**	R/W	
2	**SMB2_D2**	R/W	
1	**SMB2_D1**	R/W	
0	**SMB2_D0**	R/W	

3. FUP1/FUP1-N7F/N7E SMBus 3rd Data Register, 0x04h

Bit	Type	R/W	Description
7	**SMB3_D7**	R/W	**3rd Byte Data of SMBus :** When write operation, SMB3_D[7:0] are sent to CPU through SMBus. When read operation, SMB3_D[7:0] are received from CPU through SMBus.
6	**SMB3_D6**	R/W	
5	**SMB3_D5**	R/W	
4	**SMB3_D4**	R/W	
3	**SMB3_D3**	R/W	
2	**SMB3_D2**	R/W	
1	**SMB3_D1**	R/W	
0	**SMB3_D0**	R/W	

4. FUP1/FUP1-N7F/N7E SMBus 4th Data Register, 0x05h

Bit	Type	R/W	Description
7	**SMB4_D7**	R/W	**4th Byte Data of SMBus :** When write operation, SMB4_D[7:0] are sent to CPU through SMBus. When read operation, SMB4_D[7:0] are received from CPU through SMBus.
6	**SMB4_D6**	R/W	
5	**SMB4_D5**	R/W	
4	**SMB4_D4**	R/W	
3	**SMB4_D3**	R/W	
2	**SMB4_D2**	R/W	
1	**SMB4_D1**	R/W	
0	**SMB4_D0**	R/W	

5. FUP1/FUP1-N7F/N7E SMBus 5th Data Register, 0x06h

Bit	Type	R/W	Description
7	**SMB5_D7**	R/W	**5th Byte Data of SMBus :** When write operation, SMB5_D[7:0] are sent to CPU through SMBus. When read operation, SMB5_D[7:0] are received from CPU through SMBus.
6	**SMB5_D6**	R/W	
5	**SMB5_D5**	R/W	
4	**SMB5_D4**	R/W	
3	**SMB5_D3**	R/W	
2	**SMB5_D2**	R/W	
1	**SMB5_D1**	R/W	
0	**SMB5_D0**	R/W	

6. FUP1/FUP1-N7F/N7E SMBus 6th Data Register, 0x07h

Bit	Type	R/W	Description
7	**SMB6_D7**	R/W	**6th Byte Data of SMBus :** When write operation, SMB6_D[7:0] are sent to CPU through SMBus. When read operation, SMB6_D[7:0] are received from CPU through SMBus.
6	**SMB6_D6**	R/W	
5	**SMB6_D5**	R/W	
4	**SMB6_D4**	R/W	
3	**SMB6_D3**	R/W	
2	**SMB6_D2**	R/W	
1	**SMB6_D1**	R/W	
0	**SMB6_D0**	R/W	

7. FUP1/FUP1-N7F/N7E SMBus Control Register, 0x08h

Bit	Type	R/W	Description
7	**SLV_AR6**	R/W	**Slave Address Byte of SMBus :** Slave address assigned by microcontroller vendor support SMBus interface.
6	**SLV_AR5**	R/W	
5	**SLV_AR4**	R/W	
4	**SLV_AR3**	R/W	
3	**SLV_AR2**	R/W	
2	**SLV_AR1**	R/W	
1	**SLV_AR0**	R/W	
0	**WR**	R/W	**SMBus Read/Write Direction bit :** The direction bit is the LSB of slave address byte. 0: Write operation. 1: Read operation.

8. FUP1/FUP1-N7F/N7E SMBus Control Register, 0x09h

Bit	Type	R/W	Description
7~4	Reserved	RO	
3	**SMB_RAM**	R/W	**SMBus Register Addressing Mode :** 0 : Support 1 byte register addressing mode (default). 1 : Support 2 bytes register addressing mode.
2	**SMB_OK**	R/W	**SMBus Data Transfer Success :** 0 : SMBus data transfer is failed (default). 1 : SMBus data transfer is succeeded.
1	**SMB_CLK**	R/W	**Data Clock Select (pin C_SCL) :** Select SMBus data clock rate 0 : 100KHz clock select (default) 1 : 400KHz clock select
0	**SMB_STRT**	R/W, SC	**Data Transfer Start :** FUP1 start to transfer data which formed registers 0x02 ~ 0x08 into a SMBus data format to microcontroller. 0 : SMBus idle (default). 1 : Start to transfer data to microcontroller. **Note :** **It will be self clear after the transfer is finished.**

4.1.3 GPIO Control Register

1. FUP1/FUP1-N7F/N7E GPIO[3:0] Control Register, 0x0Ah

Bit	Type	R/W	Description
7	**GPIO_Out3**	R/W	**GPIO[3:0] Control Register :** (Default value: 0x00h) **GPIO_Out[3:0] :** GPIO [3:0] When set as output mode, value is for output, in contrast, current value will be read in input mode. **GPIO_Dir[3:0] :** GPIO[3:0] mode select 0 : Input mode 1 : Output mode
6	**GPIO_Dir3**	R/W	
5	**GPIO_Out2**	R/W	
4	**GPIO_Dir2**	R/W	
3	**GPIO_Out1**	R/W	
2	**GPIO_Dir1**	R/W	
1	**GPIO_Out0**	R/W	
0	**GPIO_Dir0**	R/W	

2. FUP1-D7F/D7E GPIO[1:0] Control Register, 0x0Ah

Bit	Type	R/W	Description
7	**GPIO_Out1**	R/W	**GPIO[1:0] Control Register :** (Default value: 0x00h) **GPIO_Out[1:0] :** GPIO [1:0] When set as output mode, value is for output, in contrast, current value will be read in input mode. **GPIO_Dir[1:0] :** GPIO[1:0] mode select 0 : Input mode 1 : Output mode
6	**GPIO_Dir1**	R/W	
5	Reserved	RO	
4	Reserved	RO	
3	Reserved	RO	
2	Reserved	RO	
1	**GPIO_Out0**	R/W	
0	**GPIO_Dir0**	R/W	

4.1.4 Interrupt Control Register

1. FUP1 Interrupt Trigger Hold Register, 0x0Bh

Bit	Type	R/W	Description
7	Reserved	RO	**Interrupt Trigger Hold Register :** Interrupt trigger hold register. Each bit is mapping to one interrupt pin respectively. INT_HOLD[4:1] 0 : No interrupt event is sampled by INT_[n] pin. 1 : interrupt event is sampled by INT_[n] pin according the setting of register 0x0C & 0x0D. **Note :** **1. n = 1 ~ 4.** **2. It will be clear by register 0x0E.**
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	**INT_HOLD4**	R/W	
2	**INT_HOLD3**	R/W	
1	**INT_HOLD2**	R/W	
0	**INT_HOLD1**	R/W	

2. FUP1-D7F/D7E/N7F/N7E Interrupt Trigger Hold Register, 0x0Bh

Bit	Type	R/W	Description
7	Reserved	RO	**Interrupt Trigger Hold Register :** Interrupt trigger hold register. Each bit is mapping to one interrupt pin respectively. INT_HOLD[2:1] 0 : No interrupt event is sampled by INT_[n] pin. 1 : interrupt event is sampled by INT_[n] pin according the setting of register 0x0C & 0x0D. **Note :** **1. n = 1 ~ 2.** **2. It will be clear by register 0x0E.**
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	**INT_HOLD2**	R/W	
2	Reserved	RO	
1	**INT_HOLD1**	R/W	
0	Reserved	RO	

3. FUP1 Interrupt Edge Trigger Register, 0x0Ch

Bit	Type	R/W	Description
7	Reserved	RO	**Interrupt Level Trigger Setting :** Interrupt level trigger setting. Each bit is mapping to one interrupt pin respectively. INT_EGTRG[4:1] 0: Set level trigger Input (default). 1: Set edge trigger input.
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	**INT_EGTRG4**	R/W	
2	**INT_EGTRG3**	R/W	
1	**INT_EGTRG2**	R/W	
0	**INT_EGTRG1**	R/W	

4. FUP1-D7F/D7E/N7F/N7E Interrupt Edge Trigger Register, 0x0Ch

Bit	Type	R/W	Description
7	Reserved	RO	**Interrupt Edge Trigger Setting :** Interrupt level trigger setting. Each bit is mapping to one interrupt pin respectively. INT_EGTRG[2:1] 0: Set level trigger Input (default). 1: Set edge trigger input.
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	**INT_EGTRG2**	R/W	
2	Reserved	RO	
1	**INT_EGTRG1**	R/W	
0	Reserved	RO	

5. FUP1 Interrupt Edge / Level Selection Register, 0x0Dh

Bit	Type	R/W	Description
7	Reserved	RO	**Interrupt Trigger Edge / Level Selection :** Interrupt trigger edge or level setting. Each bit is mapping to one interrupt pin respectively. INT_EGLS[4:1] 0: Rising edge or Level one triggered (default). 1: Falling edge or Level zero triggered.
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	**INT_EGLS4**	R/W	
2	**INT_EGLS3**	R/W	
1	**INT_EGLS2**	R/W	
0	**INT_EGLS1**	R/W	

6. FUP1-D7F/D7E/N7F/N7E Interrupt Edge / Level Selection Register, 0x0Dh

Bit	Type	R/W	Description
7	Reserved	RO	**Interrupt Trigger Edge / Level Selection :** Interrupt trigger edge or level setting. Each bit is mapping to one interrupt pin respectively. INT_EGLS[2:1] 0: Rising edge or Level one triggered (default). 1: Falling edge or Level zero triggered.
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	**INT_EGLS2**	R/W	
2	Reserved	RO	
1	**INT_EGLS1**	R/W	
0	Reserved	RO	

7. FUP1 Interrupt Trigger Reset Register, 0x0Eh

Bit	Type	R/W	Description
7	Reserved	RO	**Interrupt Trigger Reset Setting :** Interrupt trigger hold register reset setting. Each bit is mapping to one interrupt trigger hold register respectively. TRG_RST[4:1] 0: Normal operation (default). 1: Reset Interrupt trigger hold register 0x0B.
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	**TRG_RST4**	R/W	
2	**TRG_RST3**	R/W	
1	**TRG_RST2**	R/W	
0	**TRG_RST1**	R/W	

8. FUP1-D7F/D7E/N7F/N7E Interrupt Trigger Reset Register, 0x0Eh

Bit	Type	R/W	Description
7	Reserved	RO	**Interrupt Trigger Reset Setting :** Interrupt trigger hold register reset setting. Each bit is mapping to one interrupt trigger hold register respectively. TRG_RST[2:1] 0: Normal operation (default). 1: Reset Interrupt trigger hold register 0x0B.
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	**TRG_RST2**	R/W	
2	Reserved	RO	
1	**TRG_RST1**	R/W	
0	Reserved	RO	

4.1.5 EEPORM Control Register

1. FUP1/FUP1-D7F/D7E/N7F/N7E SPI EEPROM Control Register, 0x0Fh

Bit	Type	R/W	Description
7~6	Reserved	RO	
5	**EE_Reload**	R/W SC	**SPI EEPROM Reload :** Set this bit from 1 to 0 will trigger FUP1 reload from the SPI EEPROM. **Note :** **1. The SPI_EEPROM bit must be clear to enable the SPI EEPROM access.** **2. Not influenced by EE_Enable bit (bit 0).** **3. It will be self clear after the Reload is completed.**
4	**EE_Input**	R/W	**SPI EEPROM Data Input :** Read only bit, read the current **EEDI** value
3	**EE_Output**	R/W	**SPI EEPROM Data Output :** EEPROM data output value.
2	**EE_Clock**	R/W	**SPI EEPROM Clock Output :** EEPROM clock output value.
1	**EE_Chipsel**	R/W	**SPI EEPROM Chip Select Output :** EEPROM chip select output value.
0	**EE_Enable**	R/W	**SPI EEPROM Software Control Enable :** Enable SPI EEPROM software control.

4.1.6 Audio Control Register

1. FUP1/FUP1-D7F/D7E/N7F/N7E Audio Control Register, 0x10h

Bit	Type	R/W	Description
7	Reserved	RO	
6	**DWWI_PCMF**	R/W	**Dual Way Wave In PCM Format :** 0 : Dual way wave in PCM with interleaved silence audio. 1 : Dual way wave in PCM with interleaved wave out audio.
5	**DOUT_FORCE**	R/W	**Force PCM Data Output Low (DOUT pin) :** 0 : Normal operation (default). 1 : Force PCM data output low.
4	**ADSO**	R/W	**Audio Data Shift Out :** 0 : Audio data MSB shift out first (default). 1 : Audio data LSB shift out first.
3	**TRI**	R/W	**PCM Tri-state Bit 0 :** 0 : Tri-state bit 0 on positive edge of DCLK (default). 1 : Tri-state bit 0 on negative edge of DCLK.
2-1	**DF[1:0]**	R/W	**PCM Data Format :** 00 : u-Law. (default) 01 : A-Law. 10 : Reserved. 11 : Linear.
0	**RESERVED**	RO	**Must be kept as logic "0".**.

2. FUP1/FUP1-D7F/D7E/N7F/N7E PCM Receive Start Delay Control Register – Low Byte, 0x11h

Bit	Type	R/W	Description
7	**DIN_SDLY[7]**	R/W	**PCM Receive Start Delay Control Register :** (Default value: 0x00) DIN_SDLY[8:0] equals the number of DCLK following FSC before data reception begins. 0 : No delay. 1 : 1 cycle delay. **…** 511 : 511 cycle delay.
6	**DIN_SDLY[6]**	R/W	
5	**DIN_SDLY[5]**	R/W	
4	**DIN_SDLY[4]**	R/W	
3	**DIN_SDLY[3]**	R/W	
2	**DIN_SDLY[2]**	R/W	
1	**DIN_SDLY[1]**	R/W	
0	**DIN_SDLY[0]**	R/W	

Note : The programmed value must the same as the register 0x13h.

3. FUP1/FUP1-D7F/D7E/N7F/N7E PCM Receive Start Delay Control Register – High Byte, 0x12h

Bit	Type	R/W	Description
7	Reserved	RO	**PCM Receive Start Delay Control Register :** (Default value: 0x00) DIN_SDLY[8:0] equals the number of DCLK following FSC before data reception begins. 0 : No delay. 1 : 1 cycle delay. **…** 511 : 511 cycle delay.
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	Reserved	RO	
2	Reserved	RO	
1	Reserved	RO	
0	**DIN_SDLY[8]**	R/W	

Note : The programmed value must the same as the register 0x14h.

4. FUP1/FUP1-D7F/D7E/N7F/N7E PCM Transmit Start Delay Control Register – Low Byte, 0x13h

Bit	Type	R/W	Description
7	**DOUT_SDLY[7]**	R/W	**PCM Transmit Start Delay Control Register :** (Default value: 0x00) DOUT_SDLY[8:0] equals the number of DCLK following FSC before data transmission begins. 0 : No delay. 1 : 1 cycle delay. **…** 511 : 511 cycle delay.
6	**DOUT_SDLY[6]**	R/W	
5	**DOUT_SDLY[5]**	R/W	
4	**DOUT_SDLY[4]**	R/W	
3	**DOUT_SDLY[3]**	R/W	
2	**DOUT_SDLY[2]**	R/W	
1	**DOUT_SDLY[1]**	R/W	
0	**DOUT_SDLY[0]**	R/W	

Note : The programmed value must the same as the register 0x11h.

5. FUP1/FUP1-D7F/D7E/N7F/N7E PCM Transmit Start Delay Control Register – High Byte, 0x14h

Bit	Type	R/W	Description
7	Reserved	RO	**PCM Transmit Start Delay Control Register :** (Default value: 0x00) DOUT_SDLY[8:0] equals the number of DCLK following FSC before data transmission begins. 0 : No delay. 1 : 1 cycle delay. **…** 511 : 511 cycle delay.
6	Reserved	RO	
5	Reserved	RO	
4	Reserved	RO	
3	Reserved	RO	
2	Reserved	RO	
1	Reserved	RO	
0	**DOUT_SDLY[8]**	R/W	

Note : The programmed value must the same as the register 0x12h.

6. FUP1/FUP1-D7F/D7E/N7F/N7E Microphone Volume - Low Byte, 0x15h

Bit	Type	R/W	Description
7	**MPV[7]**	R/W	**Microphone Volume Value [15:0] :** There are 8 levels Volume Control as follows : 0x0D01 ~ 0x7FFF : Scale Up x 4. 0x0B01 ~ 0x0D00 : Scale Up x 3. 0x0901 ~ 0x0B00 : Scale Up x 2. 0x0701 ~ 0x0900 : No Scaling. 0x0501 ~ 0x0700 : Scale Down x 3/4. 0x0301 ~ 0x0500 : Scale Down x 1/2. 0x0000 ~ 0x0300 : Scale Down x 1/4. 0xFFFF ~ 0x8001 : Scale Down x 1/4. 0x8000 : Mute.
6	**MPV[6]**	R/W	
5	**MPV[5]**	R/W	
4	**MPV[4]**	R/W	
3	**MPV[3]**	R/W	
2	**MPV[2]**	R/W	
1	**MPV[1]**	R/W	
0	**MPV[0]**	R/W	

7. FUP1/FUP1-D7F/D7E/N7F/N7E Microphone Volume - High Byte, 0x16h

Bit	Type	R/W	Description
7	**MPV[15]**	R/W	**Microphone Volume Value [15:0] :** There are 8 levels Volume Control as follows : 0x0D01 ~ 0x7FFF : Scale Up x 4. 0x0B01 ~ 0x0D00 : Scale Up x 3. 0x0901 ~ 0x0B00 : Scale Up x 2. 0x0701 ~ 0x0900 : No Scaling. 0x0501 ~ 0x0700 : Scale Down x 3/4. 0x0301 ~ 0x0500 : Scale Down x 1/2. 0x0000 ~ 0x0300 : Scale Down x 1/4. 0xFFFF ~ 0x8001 : Scale Down x 1/4. 0x8000 : Mute.
6	**MPV[14]**	R/W	
5	**MPV[13]**	R/W	
4	**MPV[13]**	R/W	
3	**MPV[11]**	R/W	
2	**MPV[10]**	R/W	
1	**MPV[9]**	R/W	
0	**MPV[8]**	R/W	

8. FUP1/FUP1-D7F/D7E/N7F/N7E Speaker Volume - Low Byte, 0x17h

Bit	Type	R/W	Description
7	**SPV[7]**	R/W	**Speaker Volume Value [15:0] :** There are 8 levels Volume Control as follows : 0x0D01 ~ 0x7FFF : Scale Up x 4. 0x0B01 ~ 0x0D00 : Scale Up x 3. 0x0901 ~ 0x0B00 : Scale Up x 2. 0x0701 ~ 0x0900 : No Scaling. 0x0501 ~ 0x0700 : Scale Down x 3/4. 0x0301 ~ 0x0500 : Scale Down x 1/2. 0x0000 ~ 0x0300 : Scale Down x 1/4. 0xFFFF ~ 0x8001 : Scale Down x 1/4. 0x8000 : Mute.
6	**SPV[6]**	R/W	
5	**SPV[5]**	R/W	
4	**SPV[4]**	R/W	
3	**SPV[3]**	R/W	
2	**SPV[2]**	R/W	
1	**SPV[1]**	R/W	
0	**SPV[0]**	R/W	

9. FUP1/FUP1-D7F/D7E/N7F/N7E Speaker Volume - High Byte, 0x18h

Bit	Type	R/W	Description
7	**SPV[15]**	R/W	**Speaker Volume Value [15:0] :** There are 8 levels Volume Control as follows : 0x0D01 ~ 0x7FFF : Scale Up x 4. 0x0B01 ~ 0x0D00 : Scale Up x 3. 0x0901 ~ 0x0B00 : Scale Up x 2. 0x0701 ~ 0x0900 : No Scaling. 0x0501 ~ 0x0700 : Scale Down x 3/4. 0x0301 ~ 0x0500 : Scale Down x 1/2. 0x0000 ~ 0x0300 : Scale Down x 1/4. 0xFFFF ~ 0x8001 : Scale Down x 1/4. 0x8000 : Mute.
6	**SPV[14]**	R/W	
5	**SPV[13]**	R/W	
4	**SPV[13]**	R/W	
3	**SPV[11]**	R/W	
2	**SPV[10]**	R/W	
1	**SPV[9]**	R/W	
0	**SPV[8]**	R/W	

4.1.7 Serial Peripheral Interface Register

1. FUP1/FUP1-D7F/D7E/N7F/N7E Serial Peripheral Interface First Data, 0x19h

Bit	Type	R/W	Description
7	**SPI_FD7**	R/W	**Serial Peripheral Interface First Data :** Default value: 0x00 Note: 1. When writing to this register, it is the first serial peripheral interface data write byte. 2. When reading from this register, it is the first serial peripheral interface data read byte.
6	**SPI_FD6**	R/W	
5	**SPI_FD5**	R/W	
4	**SPI_FD4**	R/W	
3	**SPI_FD3**	R/W	
2	**SPI_FD2**	R/W	
1	**SPI_FD1**	R/W	
0	**SPI_FD0**	R/W	

2. FUP1/FUP1-D7F/D7E/N7F/N7E Serial Peripheral Interface Second Data, 0x1Ah

Bit	Type	R/W	Description
7	**SPI_SD7**	R/W	**Serial Peripheral Interface Second Data :** Default value: 0x00 Note: 1. When writing to this register, it is the second serial peripheral interface data write byte. 2. When reading from this register, it is the second serial peripheral interface data read byte.
6	**SPI_SD6**	R/W	
5	**SPI_SD5**	R/W	
4	**SPI_SD4**	R/W	
3	**SPI_SD3**	R/W	
2	**SPI_SD2**	R/W	
1	**SPI_SD1**	R/W	
0	**SPI_SD0**	R/W	

3. FUP1/FUP1-D7F/D7E/N7F/N7E Serial Peripheral Interface Third Data, 0x1Bh

Bit	Type	R/W	Description
7	**SPI_TD7**	R/W	**Serial Peripheral Interface Third Data :** Default value: 0x00 Note: 1. When writing to this register, it is the third serial peripheral interface data write byte. 2. When reading from this register, it is the third serial peripheral interface data read byte.
6	**SPI_TD6**	R/W	
5	**SPI_TD5**	R/W	
4	**SPI_TD4**	R/W	
3	**SPI_TD3**	R/W	
2	**SPI_TD2**	R/W	
1	**SPI_TD1**	R/W	
0	**SPI_TD0**	R/W	

4. FUP1/FUP1-D7F/D7E/N7F/N7E Serial Peripheral Interface Control Register, 0x1Ch

Bit	Type	R/W	Description
7	Reserved	RO	
6	**Byte_SEL**	R/W	**Byte Operation Select :** 0 : 2 byte transfer (default). 1 : 3 byte transfer.
5	**Xfr_Mode**	R/W	**SPI Transfer Mode :** 0 : Causes P_DOUT to tri-state on rising edge of P_CLK of LSB (default) 1 : Normal Operation; P_DOUT tri-states on rising edge of the Chip Select (/DAA_CS, /SLIC_CS or /AUX_CS).
4	**Clk_SEL2**	R/W	**Clock Speed Select :**
3	**Clk_SEL1**	R/W	
2	**Clk_SEL0**	R/W	
1	**Byte_Break**	R/W	**Break Between Byte Transfer :** 0: Chip Select pull high between byte transfer (default) 1: Continues bit transfer without byte break. **Note : Chip Select are /DAA_CS, /SLIC_CS or /AUX_CS.**

Clk_SEL2	Clk_SEL1	Clk_SEL0	Speed per cycle
0	0	0	320ns (default).
0	0	1	640ns.
0	1	0	960ns.
0	1	1	1280ns.
1	0	0	1600ns.
1	0	1	1920ns.
1	1	0	2240ns.
1	1	1	2560ns.

Bit	Type	R/W	Description
0	**Start_RW**	R/W SC	**Start Transfer or Status :** 0 : read 0 is idle (default). 1 : When write 1, it's mean to start data transfer, When read 1, indicate busy. **Note :** **1. It will be self clear after the transfer is completed.**

4.1.8 Customer ID Hold Register

1. FUP1/FUP1-D7F/D7E/N7F/N7E Customer ID Hold Register, 0x1Dh

Bit	Type	R/W	Description
7	Reserved	RO	
6~0	CID	RO	Customer ID : After power-on configuration, a 7 bits non-zero customer ID will be latched into this hold register for specific application. Default : 0x7F.

4.2EEPROM

During the EE_CS pin high, the FUP1 will access the EEPROM after hardware /RESET signal. When the EEPROM contents pass the check sum for comparison, the Vendor_ID and Product_ID will be applied. Through the SPI EEPROM Control Register, 0x0Fh, the valid serial number could be accessed. If the compared check sum of EEPROM is not a right one, no serial number will be reported. Then default ID will be applied. FUP1 supports 93C46 EEPROM interface and entry table are defined as follows.

Data Name	Address	Description	Value
Fix 00	0x00	Must be 00	00
Fix F3	0x01	Must be F3	F3
Vendor_ID (Low)	0x02	USB Vendor ID Low Byte	User Defined
Vendor_ID (High)	0x03	USB Vendor ID High Byte	User Defined
Product_ID (Low)	0x04	USB Product ID Low Byte	User Defined
Product_ID (High)	0x05	USB Product ID High Byte	User Defined
Serial_NumW0	0x06	Serial Number Byte 0	User Defined
Serial_NumW1	0x07	Serial Number Byte 1	User Defined
Serial_NumW2	0x08	Serial Number Byte 2	User Defined
Serial_NumW3	0x09	Serial Number Byte 3	User Defined
Serial_NumW4	0x0A	Serial Number Byte 4	User Defined
Serial_NumW5	0x0B	Serial Number Byte 5	User Defined
SMBus_SLA	0x0C	SMBus Slave Address	0xA0
Check Sum	0x0D	Check Sum: From Byte0 + Byte1 + Byte2 + Byte3 … + Byte12	User Defined
Manufacture String 1	0x0E	Manufacture String 1	User Defined
Manufacture String 2	0x0F	Manufacture String 2	User Defined
Manufacture String 3 …….. Manufacture String 20	0x10 …… 0x21	Manufacture String 3 …….. Manufacture String 20	User Defined
Product String 1	0x022	Product String 1	User Defined
Product String 2	0x023	Product String 2	User Defined
Product String 3 …….. Product String 20	0x24 …… 0x35	Product String 3 …….. Product String 20	User Defined

5.0 FUNCTIONAL DESCRIPTION

5.1 PCM Serial Bus

General Description

The FUP1 PCM serial bus composed of one frame synchronization clock (FSC), serial data of input (DIN) & output (DOUT), and one data clock (DCLK).

The PCM serial bus is controlled by registers. For the definite control registers access, please see 4.1 Register Tables.

DOUT data is high impedance except for the duration of the 8-bit PCM transmit.

PCM Serial Bus Data Transfer

FUP1 use USB isochronous data transfer for audio data transfer. It uses Endpoint 6 & 5 for isochronous data transfer, because isochronous transfer never halts without handshake to report a halt condition. Endpoint6 is for wave output interface and Endpoint5 is for wave input interface. Isochronous transfer is suitable for the audio data transfer, when real time audio data required.

The FUP1 support 16-bit PCM format translates to 8-bit PCM format by compressed u-Law or A-Law data formats; u-Law is more commonly used in North America and Japan, while A-Law is primarily used in Europe.

For audio control, each audio stream I/O has a USB feature unit to control the volume. By issuing the appropriate Get requests, the host software can obtain values for the volume control's attributes.

PCM Serial Bus Signal Timing

FSC signal is an 8 KHz input or output clock (pulse train signal). It enables DCLK to shift PCM data transmit or receive. PCM serial bus control can be set by register 0x00, 0x01, 0x10 to 0x14.

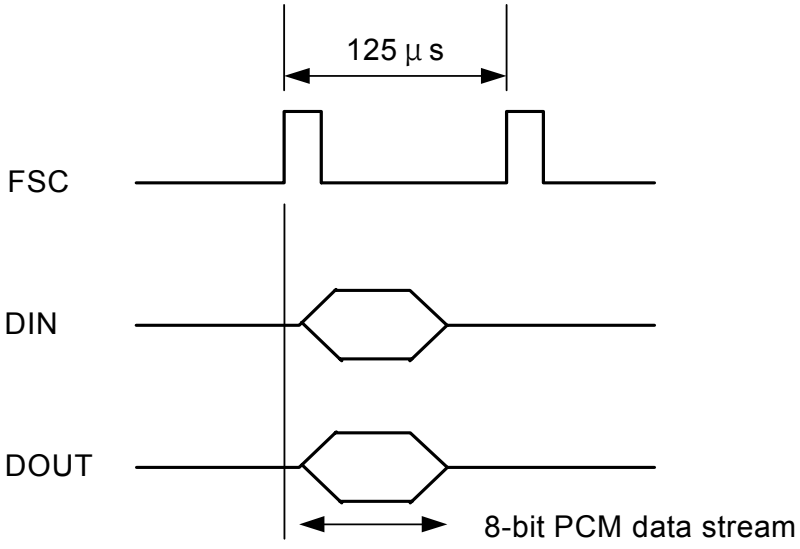


Figure 5.1 PCM Serial Bus Timing

5.2Serial Peripheral Interface (SPI)

A serial peripheral interface is used for control and configuration data transfer between peripheral devices and FUP1. SPI is a 4-wire serial bus that can be co-used such as EEPROM parameter, SLIC, DAA and Caller ID module access. And FUP1 provide 4 chip select pins for up to 4 peripheral devices connect in the system simultaneously.

SPI consists of a clock signal (P_CLK), a chip select (/DAA_CS, /SLIC_CS,EE_CS and /AUX_CS), a data output (P_DIN), & a data input (P_DOUT), it can be configured through the register 0x01. Registers 0x19 to 0x1C are used to control the SPI data transfer; ***the 8 bit contents of the register are driven out MSB first.***

For most peripheral devices, each SPI data transfer is a 2-byte transfer; the first byte of data transfer is command/address byte; the second byte is a data read or write. ***Read or write operation is defined by the MSB of first byte, 0 is for write operation and 1 is for read access***.

During the read operation, the P_DOUT will be high impedance on either the falling edge of P_CLK following the LSB, or the rising edge of Chip Select as specified by the Xfr_Mode bit of register 1C.

The P_DOUT pin will remain high impedance during write operation.

Each data read/write transfer can be programmed with or without a chip select turn around between address byte and data byte. The data clock cycle will be fixed on 320ns.

Data always transitions with the falling edge of P_CLK and is sampled on the rising edge.

The P_CLK should return to a logic high when no transfer is in progress.

5.3 USB Standard HID Command

For the system level control, the FUP1 can be accessed through USB standard HID command to the internal registers and indirectly access SLIC, DAA and Caller ID module by SPI interface. The FUP1 can only allows for single transfer in a single standard command to a single location of internal registers.

5.4 SMBus Interface

Abstract

The FUP1 can use the USB vendor command to access the internal registers (0x02 ~ 0x09) and SMBus version 1.1 compatible interfaces. For best efficiency of control transfer which support configuration/command status, the FUP1 support for multiple transfer in a single device command execution. In addition, multiple transfers can be to a single location or can increment with each transfer. ***The 8 bit contents of the register are driven out MSB first.***

For each vendor command that is issued the access timing are defined in 7.2 A.C. Characteristics.

SMBus Configuration

The FUP1 should handle SMBus interface transfer through CPU raise the interrupt signal. ***SMBus consists of bi-directional C_SCL (serial clock) and C_SDA (serial data) pins must be connected to a positive voltage through a pull-up resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the C_SCL and C_SDA lines.***

The FUP1 transmits a START and a slave address becomes the master for the duration of that transfer, and provides the serial clock pulse on C_SCL line. ***All transactions are initiated by FUP1, with one or more addressed devices as the target. No any other master device is allowed because there is no any bus arbitration scheme within the FUP1.*** Figure 5.3 shows the typical SMBus transaction.

To avoid the C_SCL line is held low by slave devices on the bus, FUP1 must detect any clock cycle held low longer than 25ms as a "timeout" condition.

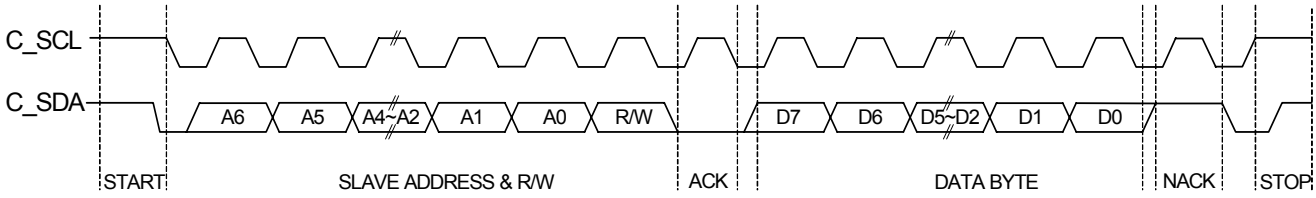


Figure 5.3 SMBus Transaction

5.5 General Purpose Input / Output

The FUP1 has 4 GPIO pins that can be set individually by registers 0x0Ah. GPIO [3:0] are bidirectional Input/Output pins.

5.6 Dual Way Audio Control Function

The FUP1 support dual way audio recording control through wave in panel user interface. Under normal operation, audio stream coming from host are wave out mono sound to speaker and microphone input to receive to host are wave in by switch to the mono state. When the dual way audio recording user panel is set by user, wave in stream are interleaved with wave out mono sound and microphone mono input to a dual-way sound to host. Switching between mono and dual-way is controlled by pin “DUAL_MONO”. See the following diagram for details.

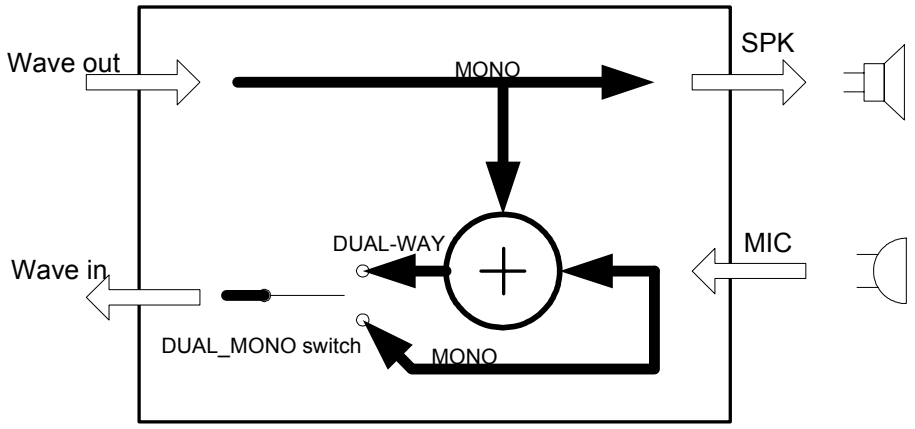
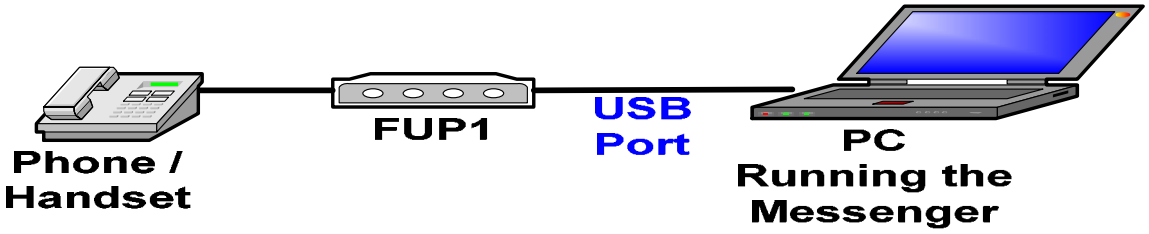


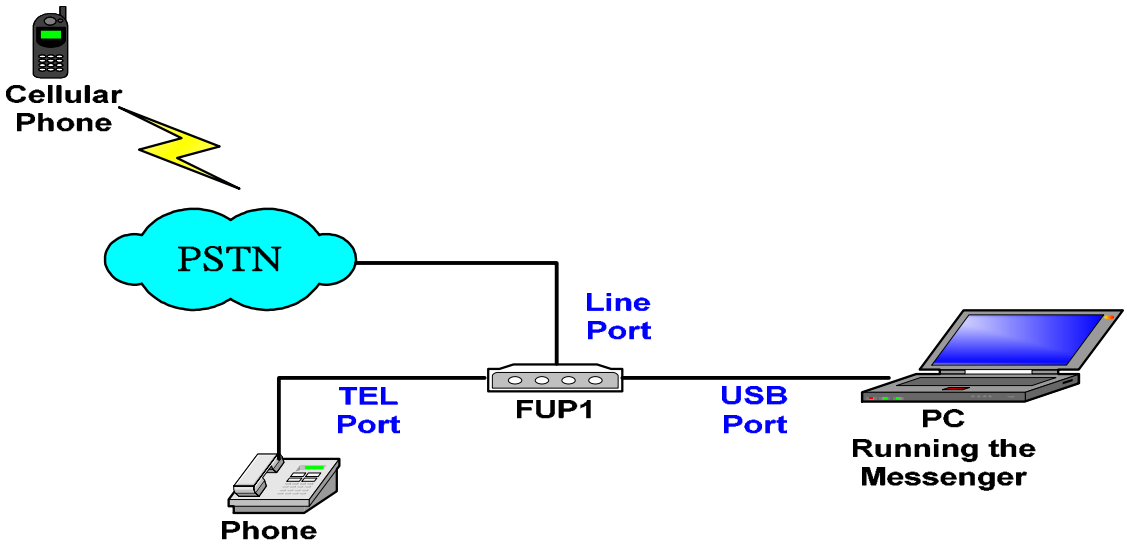
Figure 5.4 Dual Way Audio control diagram

6.0 APPLICATIONS

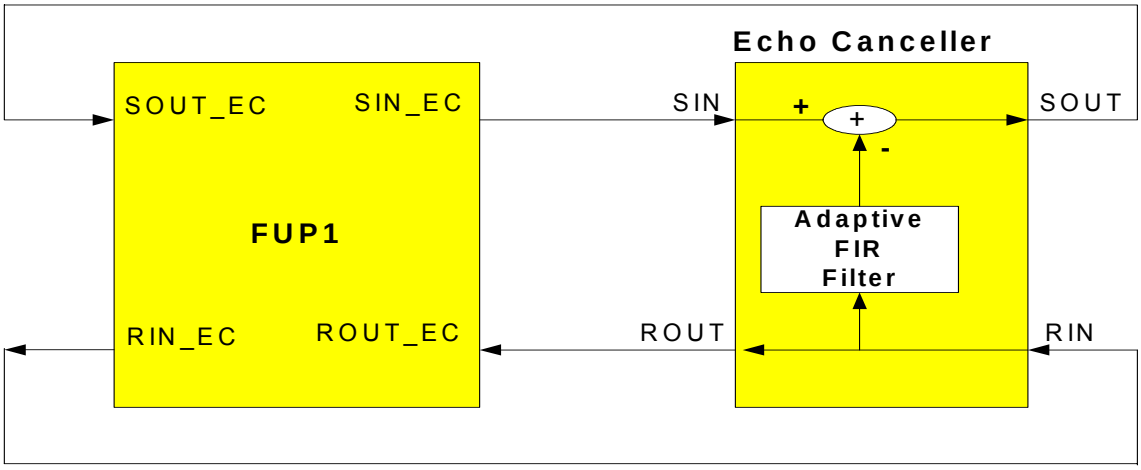
6.1 VoIP over Messenger Application



6.2 Personal Gateway Application



6.3 Echo Canceller Connection Diagram



7.0 AC and DC CHARACTERISTICS

7.1 DC Characteristics

7.1.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Core Power Supply	-0.3 to 3.9	V
V_{CC5}	Power Supply of 5V I/O	-0.3 to 6	V
V_{IN3}	Input Voltage of 3.3V I/O	-0.3 to V_{CC} + 0.3	V
	Input Voltage of 3.3V I/O with 5V tolerance	-0.3 to V_{CC5} + 0.3	
V_{OUT3}	Output Voltage of 3.3V I/O	-0.3 to V_{CC} + 0.3	V
ST	Storage Temperature	-40 ~ 150	℃
OT	Operation Temperature	-10 ~ 70	℃

Note : Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the optional sections of this datasheet. exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

7.1.2 Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Core Power Supply		3.0	3.3	3.6	V
V_{IN3}	Input Voltage of 3.3V I/O with 5V tolerance		0	3.3	5.25	V
T_j	Junction Operating Temperature	Commercial	0	25	115	℃
		Industrial	-40	25	125	

7.1.3 Capacitance

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN3}	3.3V Input Capacitance		2.8		pF
C_{OUT3}	3.3V Output Capacitance		3.3		pF
C_{BID3}	3.3V Bi-directional Capacitance		4		pF

Note : 1. The capacitance listed above does not include pad capacitance and package capacitance. You can estimate the pin capacitance by adding a pad capacitance of about 0.5pF and the package capacitance.

2. The typical capacitance listed above is for reference only. The accurate value of each I/O cell can be obtained upon request.

7.1.4 3.3V Operation

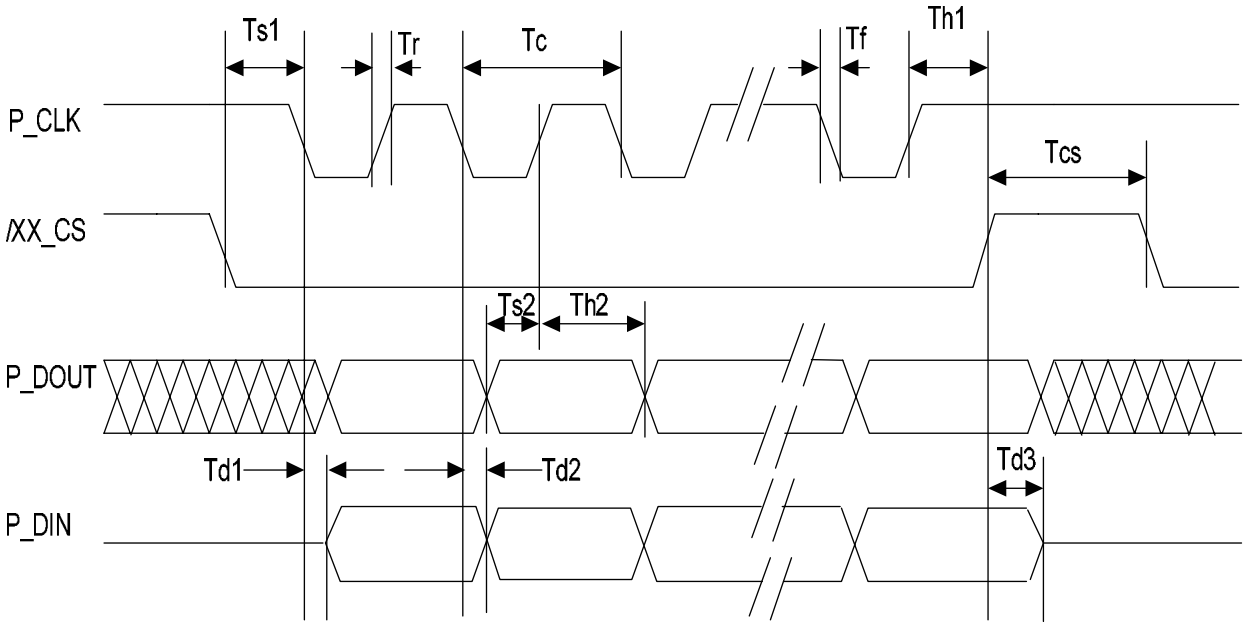
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Vcc3	Power Supply	3.3V I/O	3.0	3.3	3.6	V
V_{OH}	Output High Voltage	$I_{OH=}$ -2 ~ -24mA	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL=}$ 2 ~ 24mA	-	-	0.44	V
I_{IN}	Input Leakage Current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-State Leakage Current		-10	±1	10	μA
V_{IL}	Input Low Voltage	CMOS	-	-	0.33* Vcc	V
V_{IH}	Input High Voltage		0.7* Vcc	-	-	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage	CMOS	-	2.1	2.5	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage		0.9	1.2		V
R_{PU}	Internal Pull-Up Resistor	Vin = 0	40	75	190	KΩ
R_{PD}	Internal Pull-Down Resistor	Vin = Vcc3	40	75	190	KΩ

7.2 AC Characteristics

Note: All AC timings given are based on calculations. They are not the results of device characterization so cannot be guaranteed over temperature or supply voltage variations.

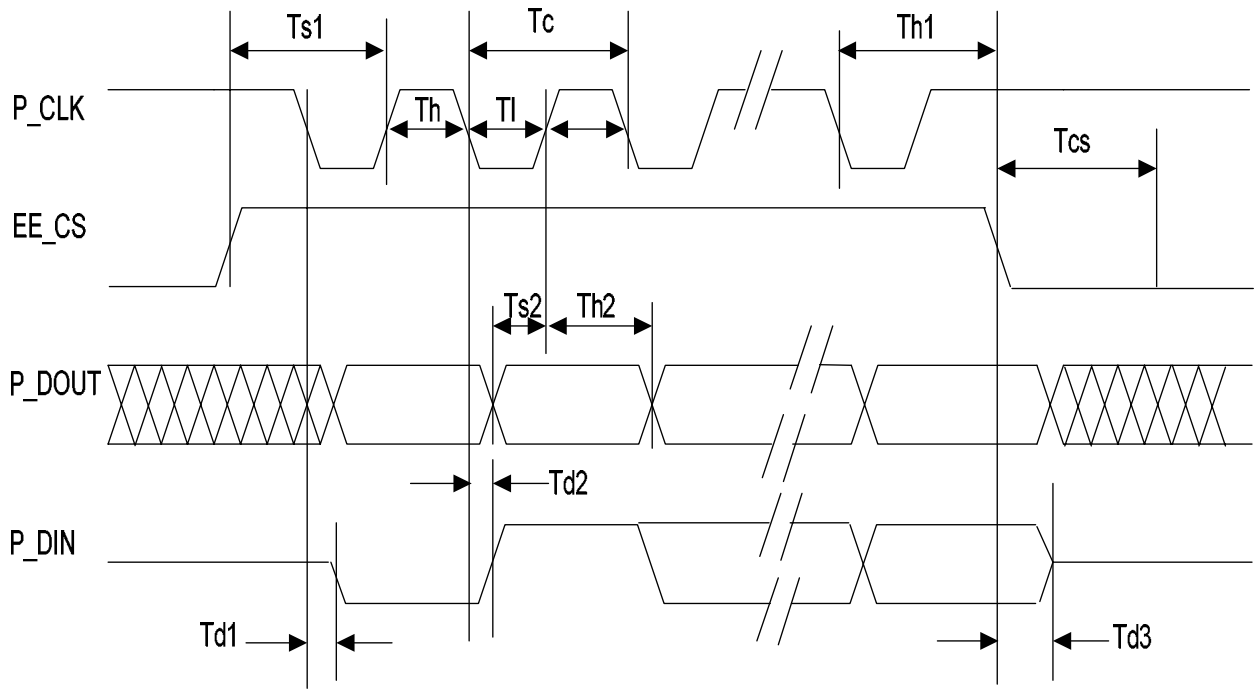
7.2.1 Serial Peripheral Interface Timing

Parameter	Description	Min	Typ	Max	Units
Tc	Cycle Time, P_CLK	0.062	-	-	us
Tr	Rise Time, P_CLK	-	-	25	ns
Tf	Fall Time, P_CLK	-	-	25	ns
Tcs	Delay Time between Chip Selects	220	-	-	ns
Ts1	Setup Time, /xx_CS to P_CLK Fall	25	-	-	ns
Th1	Hold Time, /xx_CS to P_CLK Rise	20	-	-	ns
Ts2	Setup Time, P_DOUT to P_CLK Rise	25	-	-	ns
Th2	Hold Time, P_DOUT to P_CLK Rise	20	-	-	ns
Td1	Delay Time, P_CLK fall to P_DIN Active	-	-	20	ns
Td2	Delay Time, P_CLK fall to P_DIN Transition	-	-	20	ns
Td3	Delay Time, /xx_CS rise to P_DIN Tri-State	-	-	20	ns



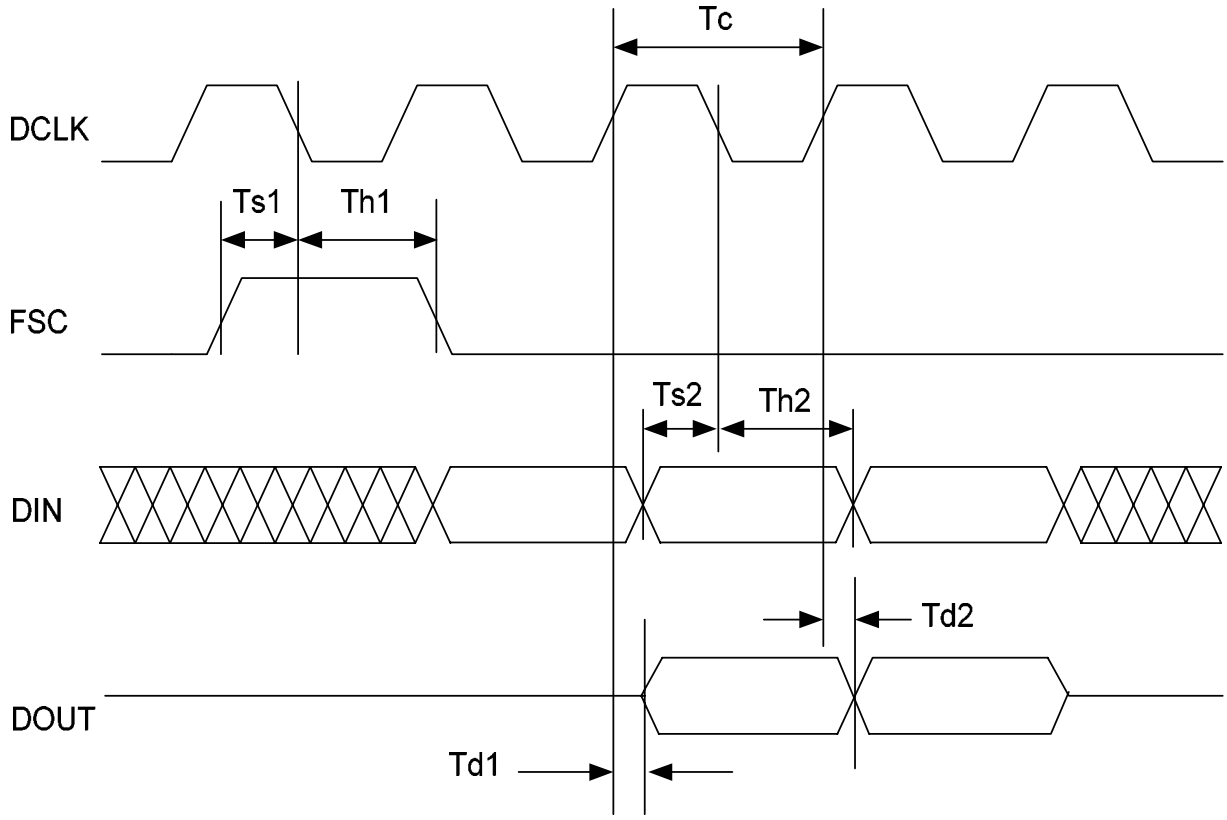
7.2.2 Serial EEPROM Interface Timing

Parameter	Description	Min	Typ	Max	Units
Tc	Cycle Time, P_CLK	1000	-	-	ns
Th	P_CLK High Time	250	-	-	ns
Tl	P_CLK Low Time	250	-	-	ns
Tcs	Minimum EE_CS Low Time	250	-	-	ns
Ts1	EE_CS Setup Time	50	-	-	ns
Th1	EE_CS Hold Time	0	-	-	ns
Ts2	Setup Time, P_DOUT to P_CLK Rise	100			ns
Th2	Hold Time, P_DOUT to P_CLK Rise	100			ns
Td1	Delay Time, P_CLK Fall to P_DIN Output “0”	-	-	250	ns
Td2	Delay Time, P_CLK Fall to P_DIN Output “1”	-	-	250	ns
Td3	Delay Time, EE_CS fall to P_DIN Tri-State	-	-	100	ns



7.2.3 PCM Interface Timing

Parameter	Description	Min	Typ	Max	Units
Tc	DCLK Frequency	- - - -	0.256 0.512 1.024 2.048	- - - -	MHz MHz MHz MHz
Ts1	Setup Time, FSC to DCLK Fall	25	-	-	ns
Th1	Hold Time, FSC to DCLK Fall	20	-	-	ns
Ts2	Setup Time, DIN to DCLK Fall	25	-	-	ns
Th2	Hold Time, DIN to DCLK Fall	20	-	-	ns
Td1	Delay Time, DCLK Rise to DOUT Active			20	ns
Td2	Delay Time, DCLK Rise to DOUT Transition			20	ns



7.2.4 SMBus Interface Timing – Standard 100KHz

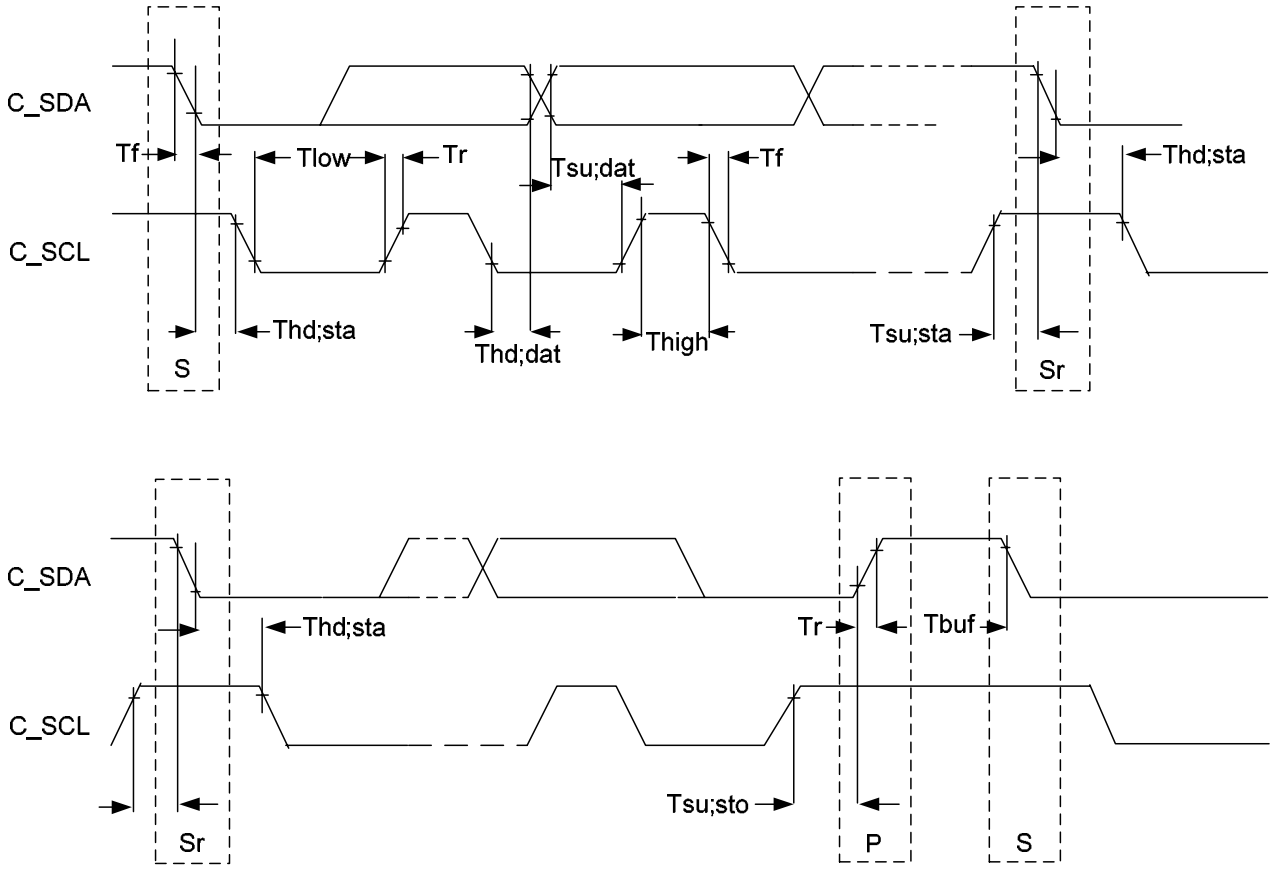
Parameter	Description	Min	Typ	Max	Units
Fsc	C_SCL clock frequency	0	-	100	KHz
Thd;sta	Hold time for a repeated START condition. After this period, the first clock pulse is generated.	4.0	-	-	us
Tlow	Low period of the C_SCL clock.	4.7	-	-	us
Thigh	High period of the C_SCL clock.	4.0	-	-	us
Tsu;sta	Set-up time for a repeated START condition.	4.7	-	-	us
Thd;dat	Data hold time	0	-	3.45	us
Tsu;dat	Data setup time.	250	-	-	ns
Tr	Rise time of both C_SDA and C_SCL signals.	-	-	1000	ns
Tf	Fall time of both C_SDA and C_SCL signals.	-	-	300	ns
Tsu;sto	Set-up time for STOP condition.	4.0	-	-	us
Tbuf	Bus free time between a STOP and START condition.	4.7	-	-	us
Cb	Capacitive load for each bus line.	-	-	400	pF

7.2.5 SMBus Interface Timing – Fast 400KHz

Parameter	Description	Min	Typ	Max	Units
Fsc	C_SCL clock frequency	0	-	400	KHz
Thd;Tsta	Hold time (repeated); START condition. After this period, the first clock pulse is generated.	0.6	-	-	us
Tlow	Low period of the C_SCL clock.	1.3	-	-	us
Thigh	High period of the C_SCL clock.	0.6	-	-	us
Tsu;sta	Set-up time for a repeated START condition.	0.6	-	-	us
Thd;dat	Data hold time.	0	-	0.9	us
Tsu;dat	Data setup time.	100	-	-	ns
Tr	Rise time of both C_SDA and C_SCL signals.	20+0.1Cb	-	300	ns
Tf	Fall time of both C_SDA and C_SCL signals.	20+0.1Cb	-	300	ns
Tsu;sto	Set-up time for STOP condition.	0.6	-	-	us
Tbuf	Bus free time between a STOP and START condition.	1.3	-	-	us
Cb	Capacitive load for each bus line.	-	-	400	pF

Notes :

1. A device must internally provide a hold time of at least 300ns for the C_SDA signal to bridge the undefined region of the falling edge of C_SCL.
2. The maximum Thd;dat has only to be met if the device does not stretch the LOW period (Tlow) of the C_SCL signal.
3. Cb = total capacitance of one bus line in pF.



7.3 Temperature Parameter

For 100 Pin PQFP

The θ_{JA} = 44.9 ℃/ W when 0 m/sec.

For 48 Pin LQFP

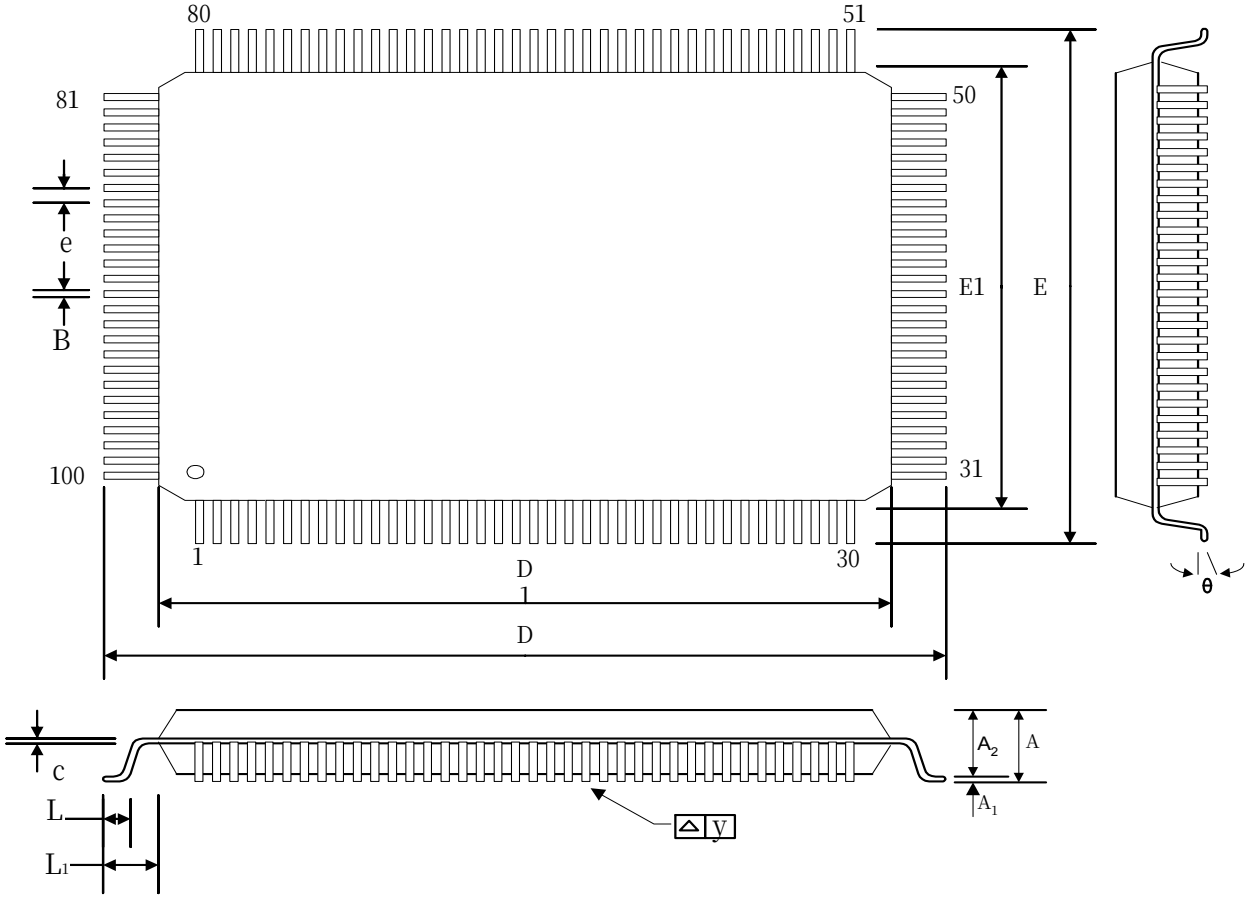
The θ_{JA} = 51.3 ℃/ W when 0 m/sec.

For 64 Pin QFN

The θ_{JA} = 25.3 ℃/ W when 0 m/sec.

8.0 PHYSICAL DIMENSIONS

8.1 100 Pin PQFP

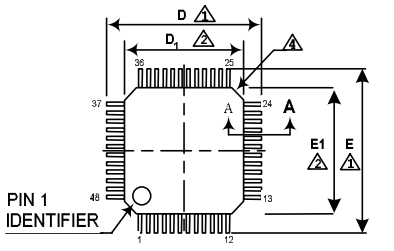


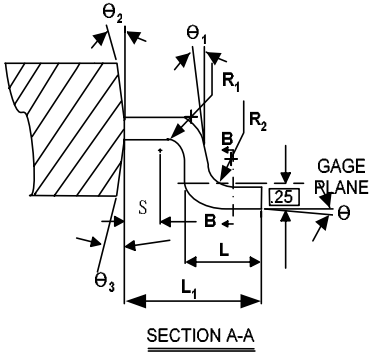
SYMBOL	Dimension in inch			Dimension in mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.130	-	-	3.30
A1	0.004	-	-	0.10	-	-
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.010	0.012	0.016	0.25	0.30	0.40
C	0.004	0.006	0.010	0.1	0.15	0.25
D	0.964	0.976	0.988	24.49	24.80	25.10
D1	0.782	0.787	0.792	19.87	20.00	20.13
E	0.728	0.740	0.752	18.49	18.80	19.10
E1	0.546	0.551	0.556	13.87	14.00	14.13
e	0.020	0.026	0.032	0.50	0.65	0.80
L	0.039	0.047	0.055	1.00	1.20	1.40
L1	0.087	0.094	0.103	2.21	2.40	2.62
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

NOTE :

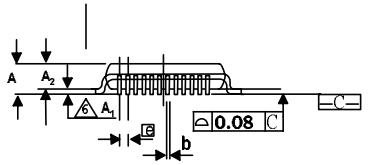
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLO PROTRUSION. BUT MOLO MISMATCH IS INCLUDED ALLOWABLE PROTRUSION IS .25mm/.010' PER SIDE.
2. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION .08mm/.003' TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
3. CONTROLLING DIMENSION : MILLIMETER.

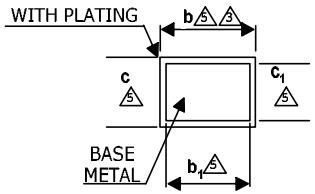
8.2 48 Pin LQFP





SECTION A-A





SECTION B-B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	——	——	1.60	——	——	0.063
A_1	0.05	——	0.15	0.002	——	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	——	0.20	0.004	——	0.008
c_1	0.09	——	0.16	0.004	——	0.006
D	9.00 BSC			0.354 BSC		
D_1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E_1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	——	——	0.003	——	——
R_2	0.08	——	0.20	0.003	——	0.008
S	0.20	——	——	0.008	——	——
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	——	——	0°	——	——
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		

NOTE:

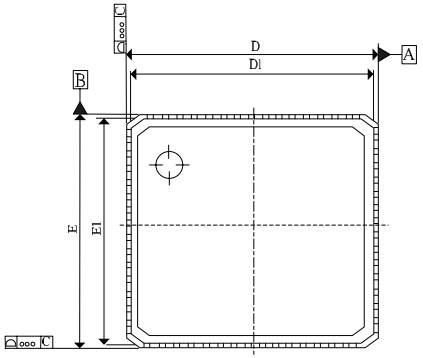
1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BBC.

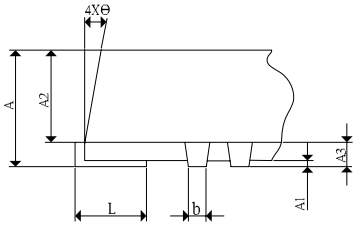
TITLE: 48LD LQFP (7*7*1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm			
L/F MATERIAL: C7025 1／2H			
APPR.		DWG NO.	
R&D		REV NO.	A
O.M		SCALE	
CHK.		DATE	JAN 17, '97
DEN.	*Eva Jiang*	SHT NO.	1/1

REV NO	DESCRIPTION	DATE

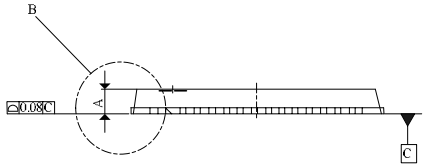
F3 Inc. TEL: 886-3-577-5535 FAX: 886-3-577-5532 http: //www.f3.com.tw
2F, NO.7, INDUSTRY E. RD.9, SCIENCE-BASE INDUSTRIAL PARK, HSINCHU, TAIWAN, R.O.C.

8.3 64 Pin QFN

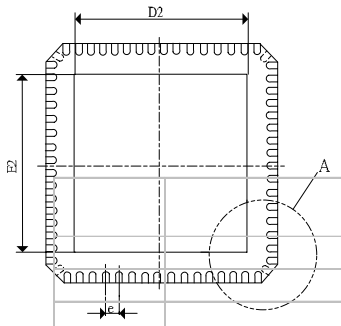


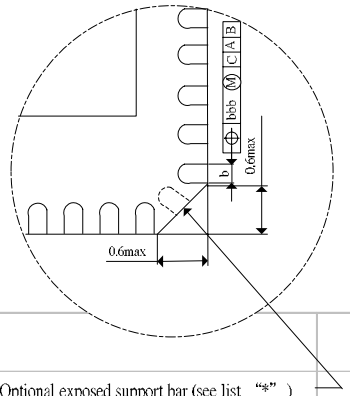


DETAIL : B



SEATING PLANE





Optional exposed support bar (see list "*")

DETAIL:A

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	0.20 REF			0.008 REF		
b	0.18	0.23	0.30	0.007	0.009	0.012
D	9.00 BSC			0.354 BSC		
D1	8.75 BSC			0.344 BSC		
E	9.00 BSC			0.354 BSC		
E1	8.75 BSC			0.344 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
Θ	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
chamfer	---	---	0.60	---	---	0.024

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENGE DOCUMENT : PROPSED JEDEC MO-220.

Exposed Pad Size & Support Bar table							
L/F	D2 (mm)			E2 (mm)			*
①	6.90	7.05	7.20	6.90	7.05	7.20	YES / NO
②	6.70	6.85	7.00	6.70	6.85	7.00	NO
③	5.54	5.69	5.84	5.54	5.69	5.84	NO
④	3.64	3.79	3.94	3.64	3.79	3.94	NO

OVER MOLD

TITLE : 64LD QFN (9x9 mm) PACKAGE OUTLINE			
L / F MATERIAL : A194 FH(PPF)			
APPR.	Holman Chen	DWG NO.	
ENG.	C.Y.Horng	REV NO.	C
QM.	S.T.Liao	PRODUCT	CE0641A
CHK.	Y.Y.Lai	DATE	06/18/'02
DWG.	R.K.Wang	SHT No.	1/1

REV NO	DESCRIPTION	DATE
C	Add Exposed Pad Size & Support bar table	06/17/02

F3 Inc. TEL: 886-3-577-5535 FAX: 886-3-577-5532 http: //www.f3.com.tw
2F, NO.7, INDUSTRY E. RD.9, SCIENCE-BASE INDUSTRIAL PARK, HSINCHU, TAIWAN, R.O.C.

9.0 REVISION HISTORY

Version	Date	Description
1.0	2005/03/31	Initial Release
1.1	2005/09/19	1. Add 48 pin LQFP Related Pin Description, Power-On Setting & Physical Dimension. 2. Add Customer ID Hold Register. 3. Remove PID, VID Power-On Configure Pins. 4. Revise the EEPROM entry table for USB manufacture string and product string descriptors. 5. Set the USB Control Register, 0x01h bit 4 as constant “0”. 6. Set the Audio Control Register, 0x10h bit 0 as constant “0”. 7. Recover SMBus Control Registers. 8. Add SMBus functional description & AC timing.
1.2	2005/10/06	Change the chip name from FUP1-D to FUP1-D7F/D7E according Marketing Dept’s naming rule conclusion.
2.0	2006/03/24	1. Add all related information for 64QFN package 2. Revise 7.2.1 SPI Timing. 3. Add 7.2.2 Serial EEPROM Interface Timing.
2.1	2006/09/14	1. Add all related information for FUP1-D7E/N7E .